Ordering number : EN*5396

CMOS LSI

# LC74751

## On-Screen Display LSI

**Preliminary**

## Overview

The LC74751 is a CMOS LSI that supports on-screen display of characters and patterns on a TV screen under the control of a microcontroller. The LC74751 includes an on-chip character ROM that provides 128 characters in a 12 × 18 dot format. This IC supports display of up to 12 lines of 24 characters each for a maximum of 288 characters.

## Features

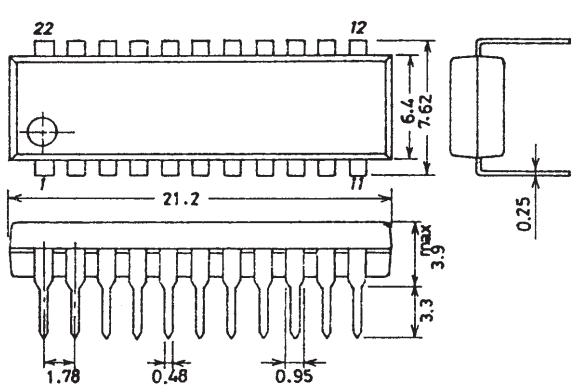
- Display format: 24 characters by 12 rows
- Characters displayed: Up to 288 characters
- Display control ROM (line ROM): ROM for 64 lines (Control in line units: lines consisting of 24 characters)
- Display RAM: 176 characters (Used for the specification of user-defined characters.)
- Character format: 12 (horizontal) × 18 (vertical) dots
- Characters in font: 128
- Character sizes: Four sizes each in the horizontal and vertical directions
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Blinking: Specifiable in character units
- Blinking types:
  - — Two periods supported: 1.0 second and 0.5 second
  - — Three duty types supported: 25%, 50%, and 75%
- Blanking: Over the whole font (12 × 18 dots)
- Background color
  - — 8 background colors (in internal synchronization mode): 4fsc (NTSC/PAL/PAL-M/PAL-N)
  - — 4 background colors (in internal synchronization mode): 2fsc (NTSC)
  - — Single background color (blue) (in internal synchronization mode): 2fsc (PAL/PAL-M/PAL-N)
- External control input: Serial data input
- Synchronizing signals: Supports switching between internal and external synchronizing signals.
- On-chip sync separator circuit
- Video output: Composite video output in the NTSC, PAL, PAL-M, or PAL-N format
- Superimpose function: Superimposes the character output on the composite video output.

## Package Dimensions

unit: mm

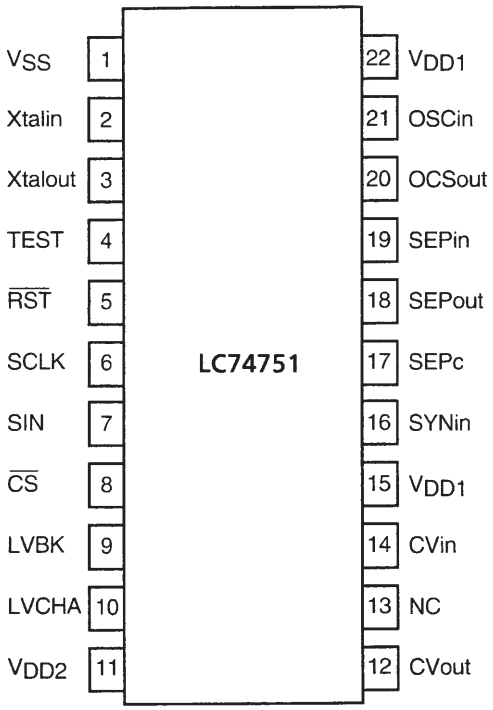
**3059-DIP22S**

[LC74751]




SANYO: DIP22S

## Pin Assignment




(Top view) A05637

# Specifications

## Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD1}$ and $V_{DD2}$ | $V_{SS}$–0.3 to $V_{SS}$+7.0 | V |
| Input voltage | $V_{IN}$ | All input pins | $V_{SS}$–0.3 to $V_{DD}$+0.3 | V |
| Output voltage | $V_{OUT}$ | | $V_{SS}$–0.3 to $V_{DD}$+0.3 | V |
| Allowable power dissipation | Pd max | Ta = 25°C | 300 | mW |
| Operating temperature | Topr | | –30 to +70 | °C |
| Storage temperature | Tstg | | –40 to +125 | °C |

## Allowable Operating Ranges

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply voltage | $V_{DD1}$ | $V_{DD1}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{DD2}$ | $V_{DD2}$ | 4.5 | 5.0 | 1.27 $V_{DD1}$ | V |
| Input high-level voltage | $V_{IH}$ | $\overline{CS}$, SIN, $\overline{RST}$, SCLK, and $SEP_{IN}$ | 0.8 $V_{DD1}$ | | $V_{DD1}$ + 0.3 | V |
| Input low-level voltage | $V_{IL}$ | $\overline{CS}$, SIN, $\overline{RST}$, SCLK, and $SEP_{IN}$ | $V_{SS}$ – 0.3 | | 0.2 $V_{DD1}$ | V |
| Composite video input voltage | $V_{IN1}$ | $CV_{IN}$ | | 2 Vp-p | | V |
| | $V_{IN2}$ | $SYN_{IN}$ | | 2 Vp-p | 2.5 Vp-p | V |
| Oscillator frequency | $f_{OSC1}$ | Crystal oscillator pins (NTSC: 2fsc mode) | | 7.15909 | | MHz |
| | $f_{OSC2}$ | Crystal oscillator pins (NTSC: 4fsc mode) | | 14.31818 | | MHz |
| | $f_{OSC3}$ | Crystal oscillator pins (PAL: 4fsc mode) | | 17.73447 | | MHz |
| | $f_{OSC4}$ | Crystal oscillator pins (PAL-M: 4fsc mode) | | 14.30244 | | MHz |
| | $f_{OSC5}$ | Crystal oscillator pins (PAL-N: 4fsc mode) | | 14.32822 | | MHz |
| | $f_{OSC6}$ | LC oscillator pin (When an LC oscillator is used) | 5 | 7 | 11 | MHz |

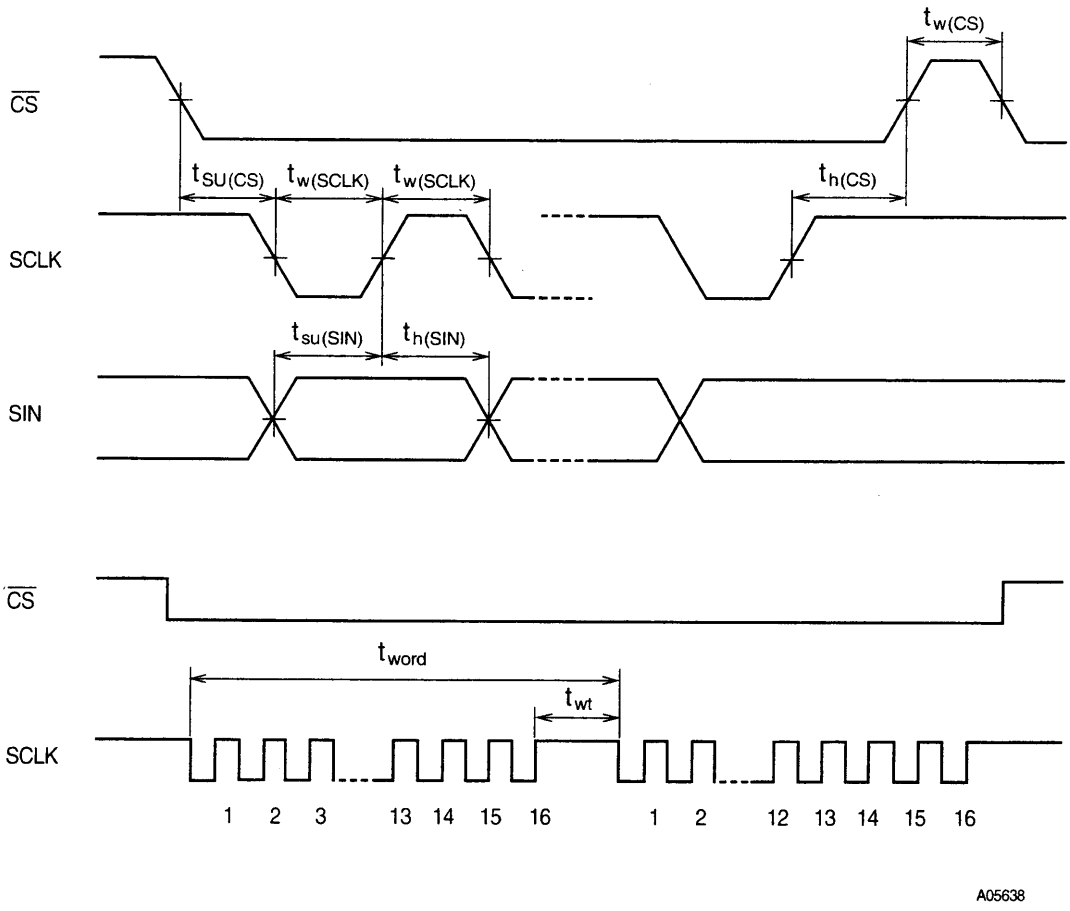
## Electrical Characteristics at Ta = –30 to +70°C, $V_{DD1}$ = 5 V unless otherwise specified

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Output off leakage current | $I_{leak}$ | $CV_{OUT}$ | | | 10 | µA |
| Output high-level voltage | $V_{OH1}$ | $SEP_{OUT}$: $V_{DD1}$ = 4.5 V, $I_{OH}$ = –1.0 mA | 3.5 | | | V |
| Output low-level voltage | $V_{OL1}$ | $SEP_{OUT}$: $V_{DD1}$ = 4.5 V, $I_{OL}$ = 1.0 mA | | | 1.0 | V |
| Input current | $I_{IH}$ | $\overline{CS}$, SIN, $\overline{RST}$, SCLK, and $SEP_{IN}$: $V_{IN}$ = $V_{DD1}$ | | | 1 | µA |
| | $I_{IL}$ | $OSC_{IN}$: $V_{IN}$ = $V_{SS}$ | –1 | | | µA |
| Operating current drain | $I_{DD1}$ | $V_{DD1}$; All outputs open, Xtal: 17.734MHz, LC = 7MHz | | | 10 | mA |
| | $I_{DD2}$ | $V_{DD2}$; $V_{DD2}$ = 5.0 V | | | 15 | mA |

## Timing Characteristics at Ta = –30 to +70°C, $V_{DD1}$ = 5±0.5 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Minimum input pulse width | $t_{W(SCLK)}$ | SCLK | 200 | | | ns |
| | $t_{W(CS)}$ | $\overline{CS}$ (the period when $\overline{CS}$ is high) | 1 | | | µs |
| Data setup time | $t_{SU(CS)}$ | $\overline{CS}$ | 200 | | | ns |
| | $t_{SU(SIN)}$ | SIN | 200 | | | ns |
| Data hold time | $t_{h(CS)}$ | $\overline{CS}$ | 2 | | | µs |
| | $t_{h(SIN)}$ | SIN | 200 | | | ns |
| One-word write time | $t_{word}$ | The time to write 16 bits of data | 10 | | | µs |
| | $t_{wt}$ | The time to write data to RAM | 1 | | | µs |

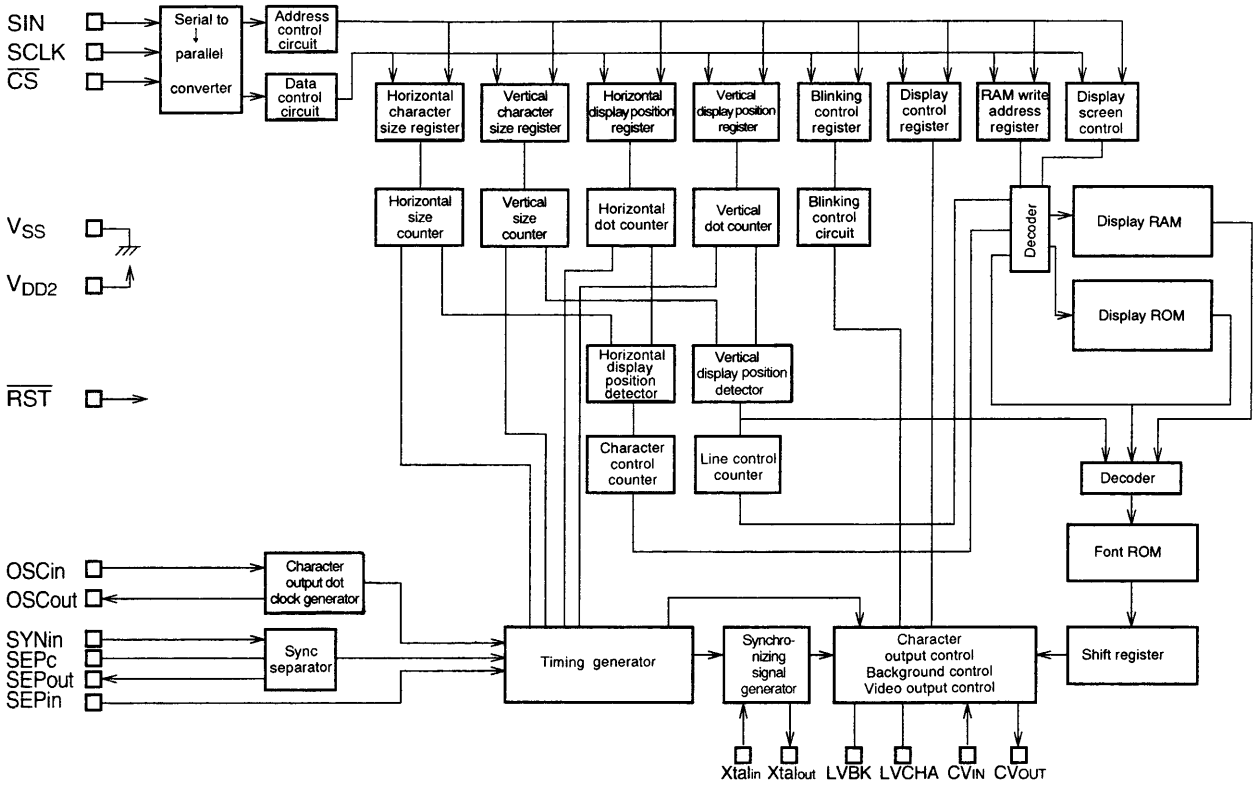
## Serial Data Input Timing



## Pin Functions

| Pin no. | Pin | Function | Notes |
|---|---|---|---|
| 1 | $V_{SS}$ | Ground | Ground (digital system ground) |
| 2 | $Xtal_{IN}$ | Crystal oscillator | Connections for the crystal and capacitors used to form the crystal oscillator for generating internal synchronizing signals. |
| 3 | $Xtal_{OUT}$ | | |
| 4 | TEST | Test output | Test data output |
| 5 | $\overline{RST}$ | Reset input | System reset input (This input has hysteresis characteristics.) |
| 6 | SCLK | Clock input | Clock input for the serial data input function (This input has hysteresis characteristics.) |
| 7 | SIN | Data input | Serial data input (This input has hysteresis characteristics.)<br>Data is input in 16-bit units. |
| 8 | $\overline{CS}$ | Enable input | Serial data input enable input (This input has hysteresis characteristics.)<br>Serial data input is enabled when this pin is low. |
| 9 | LVBK | Blanking level adjustment input | Level input signal used to adjust the blanking level. |
| 10 | LVCHA | Character level adjustment input | Level input signal used to adjust the character level. |
| 11 | $V_{DD2}$ | Power supply | Composite video signal adjustment power supply (analog system power supply) |
| 12 | $CV_{OUT}$ | Video signal output | Composite video signal output |
| 13 | NC | | This pin must be either connected to ground or left open. |
| 14 | $CV_{IN}$ | Video signal input | Composite video signal input |
| 15 | $V_{DD1}$ | Power supply | Power supply (+5 V) |
| 16 | $SYN_{IN}$ | Sync separator circuit input | Input to the composite sync signal sync separator circuit |
| 17 | $SEP_C$ | Sync separator circuit adjustment | Sync separator circuit adjustment |
| 18 | $SEP_{OUT}$ | Composite sync signal output | Sync separator circuit composite sync signal output |
| 19 | $SEP_{IN}$ | Vertical synchronizing signal input | Connect an integration circuit between the $SEP_{OUT}$ pin and this pin, which inputs the vertical synchronizing signal, to integrate the output signal from the $SEP_{OUT}$ pin. |
| 20 | $OSC_{OUT}$ | LC oscillator | Connections for the coil and capacitor that form the oscillator used to generate the character output dot clock. |
| 21 | $OSC_{IN}$ | | |
| 22 | $V_{DD1}$ | Power supply (+5 V) | Power supply (+5 V) |

## System Block Diagram




## Display Screen Structure

The display mode has a 24-character by 12-row format.

The maximum number of characters that can be displayed is 288.

When character sizes are enlarged, the maximum number of characters that can be displayed is reduced.

Display ROM (12-line specification) and display RAM (for 176 characters)

- Specify fixed characters in the display line ROM.
- Application programs use the display RAM to specify characters for sections of the display in which the characters change.

| | 24 characters | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 12 lines | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |
| | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 |
| | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 |
| | 96 | 97 | 98 | 99 | 100 | 101 | 102 | 103 | 104 | 105 | 106 | 107 | 108 | 109 | 110 | 111 | 112 | 113 | 114 | 115 | 116 | 117 | 118 | 119 |
| | 120 | 121 | 122 | 123 | 124 | 125 | 126 | 127 | 128 | 129 | 130 | 131 | 132 | 133 | 134 | 135 | 136 | 137 | 138 | 139 | 140 | 141 | 142 | 143 |
| | 144 | 145 | 146 | 147 | 148 | 149 | 150 | 151 | 152 | 153 | 154 | 155 | 156 | 157 | 158 | 159 | 160 | 161 | 162 | 163 | 164 | 165 | 166 | 167 |
| | 168 | 169 | 170 | 171 | 172 | 173 | 174 | 175 | 176 | 177 | 178 | 179 | 180 | 181 | 182 | 183 | 184 | 185 | 186 | 187 | 188 | 189 | 190 | 191 |
| | 192 | 193 | 194 | 195 | 196 | 197 | 198 | 199 | 200 | 201 | 202 | 203 | 204 | 205 | 206 | 207 | 208 | 209 | 210 | 211 | 212 | 213 | 214 | 215 |
| | 216 | 217 | 218 | 219 | 220 | 221 | 222 | 223 | 224 | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 232 | 233 | 234 | 235 | 236 | 237 | 238 | 239 |
| | 240 | 241 | 242 | 243 | 244 | 245 | 246 | 247 | 248 | 249 | 250 | 251 | 252 | 253 | 254 | 255 | 256 | 257 | 258 | 259 | 260 | 261 | 262 | 263 |
| | 264 | 265 | 266 | 267 | 268 | 269 | 270 | 271 | 272 | 273 | 274 | 275 | 276 | 277 | 278 | 279 | 280 | 281 | 282 | 283 | 284 | 285 | 286 | 287 |

## Memory Organization (display RAM and control RAM)

Both memory addresses and data are 16-bit quantities.

The locations at addresses 000 (000 hexadecimal) to 175 (0AF hexadecimal) hold display memory (RAM) data.

The locations at addresses 176 (0B0 hexadecimal) to 191 (0BF hexadecimal) hold display control register data.

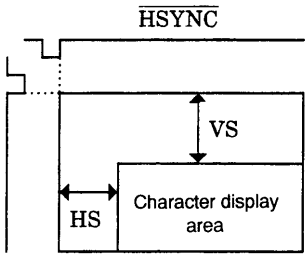
| Bit / Address | DA F | DA E | DA D | DA C | DA B | DA A | DA 9 | DA 8 | DA 7 | DA 6 | DA 5 | DA 4 | DA 3 | DA 2 | DA 1 | DA 0 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 (000h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ATTR | C6 | C5 | C4 | C3 | C2 | C1 | C0 | Display RAM |
| ↓ | | | | | | | | | ATTR | Character code | | | | | | | |
| 175 (0AFh) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ATTR | C6 | C5 | C4 | C3 | C2 | C1 | C0 | |
| 176 (0B0h) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the first line |
| 177 (0B1h) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the second line |
| 178 (0B2h) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the third line |
| 179 (0B3h) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the fourth line |
| 180 (0B4h) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the fifth line |
| 181 (0B5h) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the sixth line |
| 182 (0B6h) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the seventh line |
| 183 (0B7h) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the eighth line |
| 184 (0B8h) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the ninth line |
| 185 (0B9h) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the tenth line |
| 186 (0BAh) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the eleventh line |
| 187 (0BBh) | 0 | 0 | 0 | 0 | 0 | ADR A | ADR 9 | ADR 8 | ADR 7 | ADR 6 | ADR 5 | ADR 4 | ADR 3 | ADR 2 | ADR 1 | ADR 0 | Display line ROM specification<br>First character in the twelfth line |
| 188 (0BCh) | 0 | 0 | 0 | 0 | HSZ 31 | HSZ 30 | HSZ 21 | HSZ 20 | HSZ 11 | HSZ 10 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 | Horizontal display position<br>Horizontal character size |
| 189 (0BDh) | 0 | 0 | 0 | 0 | VSZ 31 | VSZ 30 | VSZ 21 | VSZ 20 | VSZ 11 | VSZ 10 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | Vertical display position<br>Vertical character size |
| 190 (0BEh) | 0 | 0 | 0 | 0 | $\overline{\text{INT}}$/ NON | $\overline{\text{LC}}$/ XTAL | $\overline{\text{2fsc}}$/ 4fsc | OSC STP | DSP ON | MUTE | SYS RST | SIG MD1 | SIG MD0 | PHASE 2 | PHASE 1 | PHASE 0 | Video signal and other items |
| 191 (0BFh) | 0 | 0 | 0 | 0 | TST MOD | VSN SEP | 0 | BLK 1 | BLK 0 | RVS ON | BLINK 2 | BLINK 1 | BLINK 0 | $\overline{\text{EXT}}$/ INT | CBOFF | BCOL | Control register |

Address 188 (0BC hexadecimal)

<table>
<tr><th rowspan="2">DA<br>0 to C</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>0</td><td>HP0<br>(LSB)</td><td>0<br>1</td><td rowspan="10">If HS is the horizontal start position then:<br>$HS = Tc \times (4 \sum_{n=0}^{5} 2^n HP_n)$<br>Tc: Period of the oscillator connected to OSCIN/OSCOUT in operating mode.</td><td rowspan="10">The 6 bits HP5:0 specify the horizontal display start position.<br>The weight of the low order bit is 4·Tc.</td></tr>
<tr><td>1</td><td>HP1</td><td>0<br>1</td></tr>
<tr><td>2</td><td>HP2</td><td>0<br>1</td></tr>
<tr><td>3</td><td>HP3</td><td>0<br>1</td></tr>
<tr><td>4</td><td>HP4</td><td>0<br>1</td></tr>
<tr><td>5</td><td>HP5<br>(MSB)</td><td>0<br>1</td></tr>
<tr><td>6</td><td>HSZ10</td><td>0<br>1</td><td rowspan="3">HSZ10 \ HSZ11 | 0 | 1<br>0 | 1 Tc/dot | 2 Tc/dot<br>1 | 3 Tc/dot | 4 Tc/dot</td><td rowspan="3">The horizontal character size for line 1</td></tr>
<tr><td>7</td><td>HSZ11</td><td>0<br>1</td></tr>
<tr><td>8</td><td>HSZ20</td><td>0<br>1</td><td rowspan="3">HSZ20 \ HSZ21 | 0 | 1<br>0 | 1 Tc/dot | 2 Tc/dot<br>1 | 3 Tc/dot | 4 Tc/dot</td><td rowspan="3">The horizontal character size for line 2</td></tr>
<tr><td>9</td><td>HSZ21</td><td>0<br>1</td></tr>
<tr><td>A</td><td>HSZ30</td><td>0<br>1</td><td rowspan="3">HSZ30 \ HSZ31 | 0 | 1<br>0 | 1 Tc/dot | 2 Tc/dot<br>1 | 3 Tc/dot | 4 Tc/dot</td><td rowspan="3">The horizontal character size for lines 2 through 12</td></tr>
<tr><td>B</td><td>HSZ31</td><td>0<br>1</td></tr>
</table>

Note: The states of all registers are set to zero when the IC is reset by the $\overline{RST}$ pin.

Address 189 (0BD hexadecimal)

<table>
<tr><th rowspan="2">DA<br>0 to C</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>0</td><td>VP0<br>(LSB)</td><td>0<br>1</td><td rowspan="8">If VS is the vertical display start position then:<br>$VS = H \times (4 \sum_{n=0}^{5} 2^n VP_n)$<br>H: the horizontal synchronization pulse period<br>  <br></td><td rowspan="8">The 6 bits VP5:0 specify the vertical display start position.<br>The weight of the low order bit is 4·H.</td></tr>
<tr><td>1</td><td>VP1</td><td>0<br>1</td></tr>
<tr><td>2</td><td>VP2</td><td>0<br>1</td></tr>
<tr><td>3</td><td>VP3</td><td>0<br>1</td></tr>
<tr><td>4</td><td>VP4</td><td>0<br>1</td></tr>
<tr><td>5</td><td>VP5<br>(MSB)</td><td>0<br>1</td></tr>
<tr><td>6</td><td>VSZ10</td><td>0<br>1</td><td rowspan="2">VSZ10 / VSZ11<br>0: 1 H/dot, 2 H/dot<br>1: 3 H/dot, 4 H/dot</td><td rowspan="2">The vertical character size for line 1</td></tr>
<tr><td>7</td><td>VSZ11</td><td>0<br>1</td></tr>
<tr><td>8</td><td>VSZ20</td><td>0<br>1</td><td rowspan="2">VSZ20 / VSZ21<br>0: 1 H/dot, 2 H/dot<br>1: 3 H/dot, 4 H/dot</td><td rowspan="2">The vertical character size for line 2</td></tr>
<tr><td>9</td><td>VSZ21</td><td>0<br>1</td></tr>
<tr><td>A</td><td>VSZ30</td><td>0<br>1</td><td rowspan="2">VSZ30 / VSZ31<br>0: 1 H/dot, 2 H/dot<br>1: 3 H/dot, 4 H/dot</td><td rowspan="2">The vertical character size for lines 3 through 12</td></tr>
<tr><td>B</td><td>VSZ31</td><td>0<br>1</td></tr>
</table>

Note: The states of all registers are set to zero when the IC is reset by the $\overline{RST}$ pin.

Address 190 (0BE hexadecimal)

<table>
<tr><th rowspan="2">DA<br>0 to C</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>0</td><td>PHASE0</td><td>0<br>1</td><td rowspan="3">
<table>
<tr><th rowspan="2">PHASE2</th><th rowspan="2">PHASE1</th><th rowspan="2">PHASE0</th><th colspan="2">Background color (phase)</th></tr>
<tr><th>NTSC</th><th>PAL (PAL-M, N)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>π/2</td><td>± π/2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>π</td><td>In phase</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>3π/2</td><td>∓ π/2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>In phase</td><td>±π</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>π/4</td><td>±3π/4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3π/4</td><td>±π/4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>5π/4</td><td>∓π/4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7π/4</td><td>±3π/4</td></tr>
</table>
</td><td rowspan="3">Background color<br>The phase of the background color with respect to the color burst signal.</td></tr>
<tr><td>1</td><td>PHASE1</td><td>0<br>1</td></tr>
<tr><td>2</td><td>PHASE2</td><td>0<br>1</td></tr>
<tr><td>3</td><td>SIGMD0</td><td>0<br>1</td><td rowspan="2">
<table>
<tr><th>SIGMD1</th><th>SIGMD0</th><th>Signal format</th></tr>
<tr><td>0</td><td>0</td><td>NTSC</td></tr>
<tr><td>0</td><td>1</td><td>PAL</td></tr>
<tr><td>1</td><td>0</td><td>PAL-M</td></tr>
<tr><td>1</td><td>1</td><td>PAL-N</td></tr>
</table>
</td><td rowspan="2"></td></tr>
<tr><td>4</td><td>SIGMD1</td><td>0<br>1</td></tr>
<tr><td>5</td><td>SYSRST</td><td>0</td><td></td><td rowspan="2">The IC is reset by a low level on the $\overline{CS}$ pin, and the reset state is cleared by a high level on that pin.</td></tr>
<tr><td></td><td></td><td>1</td><td>Resets all registers and turns display off.</td></tr>
<tr><td>6</td><td>MUTE</td><td>0</td><td>Normal output</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>$CV_{IN}$ is cut and $CV_{OUT}$ is fixed at the pedestal level.</td></tr>
<tr><td>7</td><td>DSPON</td><td>0</td><td>Character display off</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Character display on</td></tr>
<tr><td>8</td><td>OSCSTP</td><td>0</td><td>Crystal oscillator and LC oscillator circuits are not stopped.</td><td rowspan="2">Only valid in external synchronization mode when character display is off.</td></tr>
<tr><td></td><td></td><td>1</td><td>Stops the crystal oscillator and LC oscillator circuits.</td></tr>
<tr><td>9</td><td>$\overline{2fsc}$/<br>4fsc/</td><td>0</td><td>Clock frequency: 2fsc</td><td rowspan="2">Crystal oscillator circuit frequency</td></tr>
<tr><td></td><td></td><td>1</td><td>Clock frequency: 4fsc</td></tr>
<tr><td>A</td><td>$\overline{LC}$/<br>XTAL</td><td>0</td><td>The LC oscillator is used for the dot clock.</td><td rowspan="2">The $OSC_{IN}$ pin must be tied to $V_{DD}$ if the LC oscillator circuit is not used.</td></tr>
<tr><td></td><td></td><td>1</td><td>The crystal oscillator is used for the dot clock.</td></tr>
<tr><td>B</td><td>$\overline{INT}$/<br>NON</td><td>0</td><td>Interlaced (262.5 H per field: NTSC, 312.5 H per field: PAL)</td><td rowspan="2">Switches interlaced and noninterlaced display.</td></tr>
<tr><td></td><td></td><td>1</td><td>Noninterlaced (263 H per field: NTSC, 313 H per field: PAL)</td></tr>
</table>

Note: The states of all registers are set to zero when the IC is reset by the $\overline{RST}$ pin.

Address 191 (0BF hexadecimal)

<table>
<tr><th rowspan="2">DA<br>0 to C</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BCOL</td><td>0</td><td>Background color provided (only valid in internal synchronization mode)</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>No background color (Only the background level is set)</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">CBOFF</td><td>0</td><td>The burst signal is always output.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>The burst signal is not output when BCOL is high.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">$\overline{\text{EXT}}$/<br>INT</td><td>0</td><td>External synchronization</td><td rowspan="2">Switches between external and internal sources for the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ signals.</td></tr>
<tr><td>1</td><td>Internal synchronization</td></tr>
<tr><td rowspan="4">3<br>4</td><td rowspan="2">BLINK0</td><td>0</td><td rowspan="4"><table><tr><th>BLINK1 \ BLINK0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Blinking off</td><td>25% duty</td></tr><tr><td>1</td><td>50% duty</td><td>75% duty</td></tr></table></td><td rowspan="4">Changes the blinking duty ratio.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">BLINK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BLINK2</td><td>0</td><td>Blinking period: 0.5 s</td><td rowspan="2">Changes the blinking period.</td></tr>
<tr><td>1</td><td>Blinking period: 1.0 s</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">RVSON</td><td>0</td><td>Reverse video off</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Reverse video on</td></tr>
<tr><td rowspan="4">7<br>8</td><td rowspan="2">BLK0</td><td>0</td><td rowspan="4"><table><tr><th>BLK1 \ BLK0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Blinking off</td><td>Character size</td></tr><tr><td>1</td><td>Frame size</td><td>Whole area size</td></tr></table></td><td rowspan="4">Changes the blanking size</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">BLK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">—</td><td>0</td><td></td><td rowspan="2"></td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">VSNSEP</td><td>0</td><td>External V input used ($SEP_{IN}$: pin 19)</td><td rowspan="2">Selects V input when superimpose mode is used.</td></tr>
<tr><td>1</td><td>Internal V separation circuit used</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">TSTMOD</td><td>0</td><td>Normal operating mode</td><td rowspan="2">This bit must be set to 0.</td></tr>
<tr><td>1</td><td>Test mode</td></tr>
</table>

Note: The states of all registers are set to zero when the IC is reset by the $\overline{\text{RST}}$ pin.

## Memory (Display ROM) Organization

This memory has addresses ranging from 0 (000 hexadecimal) to 1535 (5FF hexadecimal).

Data has 8 bits.

| Bit / Address | DA F | DA E | DA D | DA C | DA B | DA A | DA 9 | DA 8 | DA 7 | DA 6 | DA 5 | DA 4 | DA 3 | DA 2 | DA 1 | DA 0 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 (000h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $\overline{\text{ROM}}$/RAM | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 | Line ROM: First character in the first line |
| ↓ | | | | | | | | | | | | | | | | | |
| 0023 (017h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $\overline{\text{ROM}}$/RAM | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 | Line ROM: 24th character in the first line |
| 0024 (018h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $\overline{\text{ROM}}$/RAM | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 | Line ROM: First character in the second line |
| ↓ | | | | | | | | | $\overline{\text{ROM}}$/RAM | Character code | | | | | | | |
| 1535 (5FFh) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $\overline{\text{ROM}}$/RAM | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 | Line ROM: 24th character in the 64th line |

| DA 0 to 8 | Register | Contents | | Notes |
|---|---|---|---|---|
| | | State | Function | |
| 0 | ADR0 | 0 | Specifies an address in character ROM.<br>When specifying display control RAM, DA7 must be set to 1 and ADR0 to ADR6 must be set to 0.<br>The address specification range for character ROM is 0 to 127 (7F hexadecimal). | |
| | | 1 | | |
| 1 | ADR1 | 0 | | |
| | | 1 | | |
| 2 | ADR2 | 0 | | |
| | | 1 | | |
| 3 | ADR3 | 0 | | |
| | | 1 | | |
| 4 | ADR4 | 0 | | |
| | | 1 | | |
| 5 | ADR5 | 0 | | |
| | | 1 | | |
| 6 | ADR6 | 0 | | |
| | | 1 | | |
| 7 | $\overline{\text{ROM}}$/RAM | 0 | Data is read directly from character ROM. | |
| | | 1 | Data is read from character ROM through RAM. | |

## Display Line ROM: Line Address Table

| Line no. | Address | Line no. | Address |
|---|---|---|---|
| Line 1 | $000_{HEX}$ (0000) | Line 33 | $300_{HEX}$ (0768) |
| Line 2 | $018_{HEX}$ (0024) | Line 34 | $318_{HEX}$ (0792) |
| Line 3 | $030_{HEX}$ (0048) | Line 35 | $330_{HEX}$ (0816) |
| Line 4 | $048_{HEX}$ (0072) | Line 36 | $348_{HEX}$ (0840) |
| Line 5 | $060_{HEX}$ (0096) | Line 37 | $360_{HEX}$ (0864) |
| Line 6 | $078_{HEX}$ (0120) | Line 38 | $378_{HEX}$ (0888) |
| Line 7 | $090_{HEX}$ (0144) | Line 39 | $390_{HEX}$ (0912) |
| Line 8 | $0A8_{HEX}$ (0168) | Line 40 | $3A8_{HEX}$ (0936) |
| Line 9 | $0C0_{HEX}$ (0129) | Line 41 | $3C0_{HEX}$ (0960) |
| Line 10 | $0D8_{HEX}$ (0216) | Line 42 | $3D8_{HEX}$ (0984) |
| Line 11 | $0F0_{HEX}$ (0240) | Line 43 | $3F0_{HEX}$ (1008) |
| Line 12 | $108_{HEX}$ (0264) | Line 44 | $408_{HEX}$ (1032) |
| Line 13 | $120_{HEX}$ (0288) | Line 45 | $420_{HEX}$ (1056) |
| Line 14 | $138_{HEX}$ (0312) | Line 46 | $438_{HEX}$ (1080) |
| Line 15 | $150_{HEX}$ (0336) | Line 47 | $450_{HEX}$ (1104) |
| Line 16 | $168_{HEX}$ (0360) | Line 48 | $468_{HEX}$ (1128) |
| Line 17 | $180_{HEX}$ (0384) | Line 49 | $480_{HEX}$ (1152) |
| Line 18 | $198_{HEX}$ (0408) | Line 50 | $498_{HEX}$ (1176) |
| Line 19 | $1B0_{HEX}$ (0432) | Line 51 | $4B0_{HEX}$ (1200) |
| Line 20 | $1C8_{HEX}$ (0456) | Line 52 | $4C8_{HEX}$ (1224) |
| Line 21 | $1E0_{HEX}$ (0480) | Line 53 | $4E0_{HEX}$ (1248) |
| Line 22 | $1F8_{HEX}$ (0504) | Line 54 | $4F8_{HEX}$ (1272) |
| Line 23 | $210_{HEX}$ (0528) | Line 55 | $510_{HEX}$ (1296) |
| Line 24 | $228_{HEX}$ (0552) | Line 56 | $528_{HEX}$ (1320) |
| Line 25 | $240_{HEX}$ (0576) | Line 57 | $540_{HEX}$ (1344) |
| Line 26 | $258_{HEX}$ (0600) | Line 58 | $558_{HEX}$ (1368) |
| Line 27 | $270_{HEX}$ (0624) | Line 59 | $570_{HEX}$ (1392) |
| Line 28 | $288_{HEX}$ (0648) | Line 60 | $588_{HEX}$ (1416) |
| Line 29 | $2A0_{HEX}$ (0672) | Line 61 | $5A0_{HEX}$ (1440) |
| Line 30 | $2B8_{HEX}$ (0696) | Line 62 | $5B8_{HEX}$ (1464) |
| Line 31 | $2D0_{HEX}$ (0720) | Line 63 | $5D0_{HEX}$ (1488) |
| Line 32 | $2E8_{HEX}$ (0744) | Line 64 | $5E8_{HEX}$ (1512) |

## Display Screen Structure (Display Example)

Specify the display of line 12 for display line ROM (64 lines).

From within line ROM, specify display control RAM for the sections where the characters are variable.

The addresses in display control RAM are automatically allocated in display order from 0 to 175 (AF hexadecimal).

Items enclosed in thick lines specify characters in display control RAM, and

items enclosed in thin lines are character specified in line ROM.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ROM 000 00h | ROM 001 01h | ROM 002 02h | ROM 003 03h | ROM 004 04h | ROM 005 05h | ROM 006 06h | ROM 007 07h | ROM 008 08h | ROM 009 09h | ROM 010 0Ah | ROM 011 0Bh | ROM 012 0Ch | ROM 013 0Dh | ROM 014 0Eh | ROM 015 0Fh | RAM 000 00H | RAM 001 01H | RAM 002 02H | RAM 003 03H | RAM 004 04H | RAM 005 05H | ROM 022 16h | ROM 023 17h |
| 2 | ROM 024 18h | RAM 006 06H | RAM 007 07H | RAM 008 08H | RAM 009 09H | ROM 029 1Dh | ROM 030 1Eh | ROM 031 1Fh | ROM 032 20h | ROM 033 21h | RAM 010 0AH | RAM 011 0BH | RAM 012 0CH | RAM 013 0DH | RAM 014 0EH | RAM 015 0FH | ROM 040 28h | ROM 041 29h | ROM 042 2Ah | ROM 043 2Bh | ROM 044 2Ch | ROM 045 2Dh | ROM 046 2Eh | ROM 047 2Fh |
| 3 | ROM 048 18h | RAM 016 10H | RAM 017 11H | RAM 018 12H | RAM 019 13H | RAM 020 14H | ROM 054 36h | ROM 055 37h | ROM 056 38h | ROM 057 39h | RAM 021 15H | RAM 022 16H | RAM 023 17H | RAM 024 18H | RAM 025 19H | RAM 026 1AH | RAM 027 1BH | RAM 028 1CH | RAM 029 1DH | RAM 030 1EH | ROM 068 44h | ROM 069 45h | ROM 070 46h | ROM 071 47h |
| 4 | ROM 072 48h | ROM 073 49h | ROM 074 4ah | ROM 075 4bh | ROM 076 4ch | RAM 021 1FH | RAM 032 20H | RAM 033 21H | RAM 034 22H | ROM 081 51h | RAM 035 23H | RAM 036 24H | ROM 084 54h | RAM 037 25H | RAM 038 26H | ROM 084 54h | RAM 039 27H | RAM 040 28H | ROM 090 5Ah | ROM 091 5Bh | ROM 092 5Ch | ROM 093 5Dh | ROM 094 5Eh | ROM 095 5Fh |
| 5 | ROM 096 60h | RAM 041 29H | RAM 042 2AH | RAM 043 2BH | RAM 044 2CH | RAM 045 2DH | RAM 046 2EH | RAM 047 2FH | RAM 048 30H | ROM 105 69h | RAM 049 31H | RAM 050 32H | ROM 108 6Ch | RAM 051 33H | RAM 052 34H | ROM 111 6Fh | RAM 053 35H | RAM 054 36H | ROM 114 72h | ROM 115 73h | ROM 116 74h | ROM 117 75h | ROM 118 76h | ROM 119 77h |
| 6 | ROM 120 78h | RAM 055 37H | RAM 056 38H | RAM 057 39H | RAM 058 3AH | RAM 059 3BH | RAM 060 3CH | RAM 061 3DH | ROM 128 80h | RAM 062 3EH | RAM 063 3FH | RAM 064 40H | RAM 065 41H | ROM 133 85h | RAM 066 42H | RAM 067 43H | RAM 068 44H | RAM 069 45H | RAM 070 46H | ROM 139 8Bh | RAM 071 47H | RAM 072 48H | ROM 142 8Eh | ROM 143 8Fh |
| 7 | RAM 073 49H | RAM 074 4AH | RAM 075 4BH | RAM 076 4CH | RAM 077 4DH | RAM 078 4EH | RAM 079 4FH | RAM 080 50H | RAM 081 51H | RAM 082 52H | RAM 083 53H | RAM 084 54H | ROM 156 9Ch | ROM 157 9Dh | ROM 158 9Eh | ROM 159 9Fh | ROM 160 A0h | ROM 161 A1h | ROM 162 A2h | ROM 163 A3h | ROM 164 A4h | ROM 165 A5h | ROM 166 A6h | ROM 167 A7h |
| 8 | RAM 085 55H | RAM 086 56H | RAM 087 57H | RAM 088 58H | RAM 089 59H | RAM 090 5AH | RAM 091 5BH | RAM 092 5CH | RAM 093 5DH | RAM 094 5EH | RAM 095 5FH | RAM 096 60H | ROM 180 B4h | ROM 181 B5h | ROM 182 B6h | ROM 183 B7h | ROM 184 B8h | ROM 185 B9h | ROM 186 BAh | ROM 187 BBh | ROM 188 BCh | ROM 189 BDh | ROM 190 BEh | ROM 191 BFh |
| 9 | ROM 192 C0h | ROM 193 C1h | ROM 194 C2h | ROM 195 C3h | ROM 196 C4h | ROM 197 C5h | ROM 198 C6h | ROM 199 C7h | ROM 200 C8h | ROM 201 C9h | ROM 202 CAh | ROM 203 CBh | RAM 097 61H | RAM 098 62H | RAM 099 63H | RAM 100 64H | RAM 101 65H | RAM 102 66H | RAM 103 67H | RAM 104 68H | RAM 105 69H | RAM 106 6AH | RAM 107 6BH | RAM 108 6CH |
| 10 | ROM 216 D8h | ROM 217 D9h | ROM 218 DAh | ROM 219 DBh | ROM 220 DCh | RAM 109 6DH | RAM 110 6EH | RAM 111 6FH | RAM 112 70H | RAM 113 71H | RAM 114 72H | RAM 115 73H | RAM 116 74H | RAM 117 75H | RAM 118 76H | RAM 119 77H | RAM 120 78H | RAM 121 79H | RAM 122 7AH | ROM 235 EBh | ROM 236 ECh | ROM 237 EDh | ROM 238 EEh | ROM 239 EFh |
| 11 | ROM 240 F0h | ROM 241 F1h | ROM 242 F2h | ROM 243 F3h | ROM 244 F4h | ROM 245 F5h | ROM 246 F6h | ROM 247 F7h | ROM 248 F8h | ROM 249 F9h | ROM 250 FAh | ROM 251 FBh | ROM 252 FCh | ROM 253 FDh | ROM 254 FEh | RAM 123 7BH | RAM 124 7CH | ROM 257 101h | RAM 125 7DH | RAM 126 7EH | ROM 260 104h | RAM 127 7FH | RAM 128 80H | ROM 263 107h |
| 12 | RAM 129 81H | RAM 130 82H | RAM 131 83H | RAM 132 84H | RAM 133 85H | RAM 134 86H | RAM 135 87H | RAM 136 88H | RAM 137 89H | RAM 138 8AH | RAM 139 8BH | RAM 140 8CH | RAM 141 8DH | RAM 142 8EH | RAM 143 8FH | RAM 144 90H | RAM 145 91H | RAM 146 92H | RAM 147 93H | RAM 148 94H | RAM 149 95H | RAM 150 96H | RAM 151 97H | ROM 287 11Fh |

## Control Data External Input Timing

Data is input in a 16-bit serial format that includes both an address and data items.

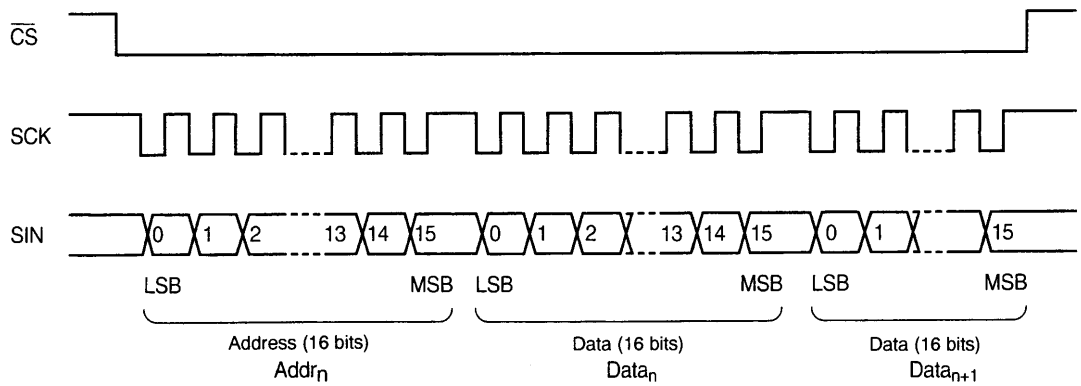
①An address has 16 bits.

The lower 8 bits are the valid address bits. The upper 8 bits must be set to 0.

②Data consists of 16 bits.

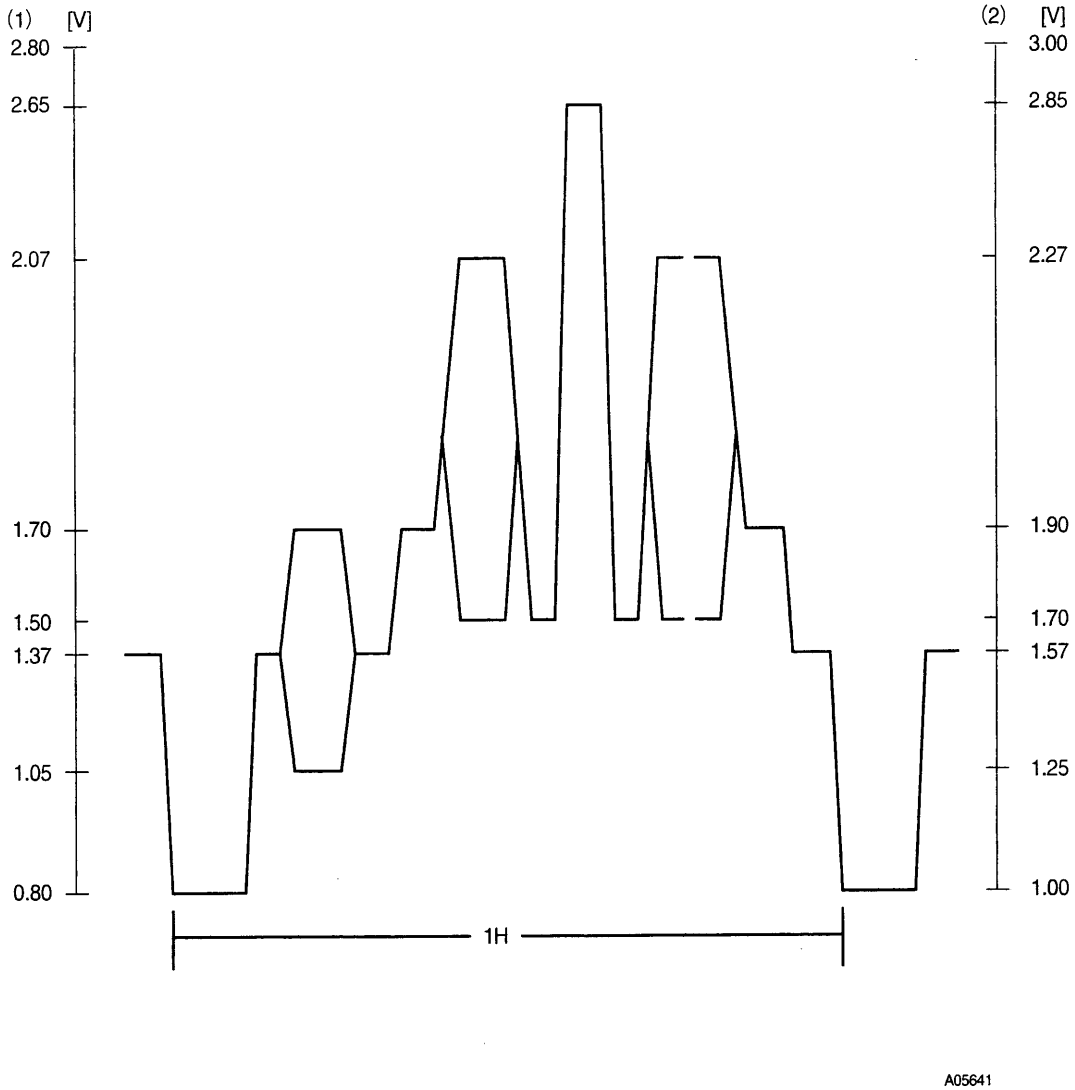
- For addresses 000 to 0AF (hexadecimal) the lower 8 bits are valid data. The upper 8 bits must be set to 0.
- For addresses 0B0 to 0BB (hexadecimal) the lower 11 bits are valid data. The upper 5 bits must be set to 0.
- For addresses 0BC to 0BF (hexadecimal) the lower 12 bits are valid data. The upper 4 bits must be set to 0.

③When data is input, the first 16 bits after the fall of the $\overline{CS}$ signal are acquired as the address, and then data is acquired in 16-bit units. The address is automatically incremented ever 16 bits.



## Composite Video Signal Output Levels (Internally Generated Levels)

$CV_{OUT}$ output level waveform ($V_{DD}2$ = 5.00 V)




| Output level | Output voltage (1) ($V_{DC}$) | Output voltage (2) ($V_{DC}$) |
|---|---|---|
| $V_{CHA}$: Character | 2.650 | 2.875 |
| $V_{RSH}$: Background color high | 2.075 | 2.275 |
| $V_{CBH}$: Color burst high | 1.700 | 1.900 |
| $V_{RSL}$: Background color low | 1.500 | 1.700 |
| $V_{BK}$: Frame | 1.500 | 1.700 |
| $V_{PD}$: Pedestal level | 1.375 | 1.575 |
| $V_{CBL}$: Color burst low | 1.050 | 1.250 |
| $V_{SN}$: Sync | 0.800 | 1.000 |

$V_{DD}2 = 5.000V_{DC}$

## Application Circuit Example