

**LC74751****On-Screen Display LSI****Preliminary****Overview**

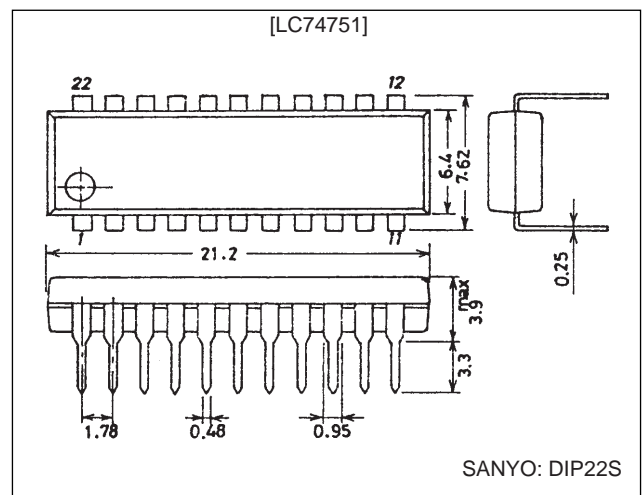
The LC74751 is a CMOS LSI that supports on-screen display of characters and patterns on a TV screen under the control of a microcontroller. The LC74751 includes an on-chip character ROM that provides 128 characters in a 12 × 18 dot format. This IC supports display of up to 12 lines of 24 characters each for a maximum of 288 characters.

**Features**

- Display format: 24 characters by 12 rows
- Characters displayed: Up to 288 characters
- Display control ROM (line ROM): ROM for 64 lines (Control in line units: lines consisting of 24 characters)
- Display RAM: 176 characters (Used for the specification of user-defined characters.)
- Character format: 12 (horizontal) × 18 (vertical) dots
- Characters in font: 128
- Character sizes: Four sizes each in the horizontal and vertical directions
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Blinking: Specifiable in character units
- Blinking types:
  - Two periods supported: 1.0 second and 0.5 second
  - Three duty types supported: 25%, 50%, and 75%
- Blanking: Over the whole font (12 × 18 dots)
- Background color
  - 8 background colors (in internal synchronization mode): 4fsc (NTSC/PAL/PAL-M/PAL-N)
  - 4 background colors (in internal synchronization mode): 2fsc (NTSC)
  - Single background color (blue) (in internal synchronization mode): 2fsc (PAL/PAL-M/PAL-N)
- External control input: Serial data input
- Synchronizing signals: Supports switching between internal and external synchronizing signals.
- On-chip sync separator circuit
- Video output: Composite video output in the NTSC, PAL, PAL-M, or PAL-N format
- Superimpose function: Superimposes the character output on the composite video output.

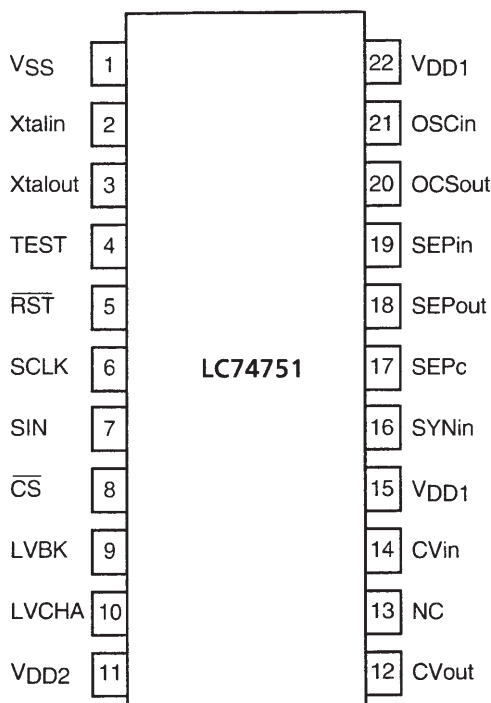
**Package Dimensions**

unit: mm

**3059-DIP22S**

## LC74751

### Pin Assignment



(Top view) A05637

### Specifications

#### Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$	$V_{DD1}$ and $V_{DD2}$	$V_{SS}-0.3$ to $V_{SS}+7.0$	V
Input voltage	$V_{IN}$	All input pins	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output voltage	$V_{OUT}$		$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Allowable power dissipation	$P_d$ max	$T_a = 25^\circ\text{C}$	300	mW
Operating temperature	$T_{opr}$		-30 to +70	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$

#### Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD1}$	$V_{DD1}$	4.5	5.0	5.5	V
	$V_{DD2}$	$V_{DD2}$	4.5	5.0	$1.27 V_{DD1}$	V
Input high-level voltage	$V_{IH}$	$\overline{CS}$ , SIN, $\overline{RST}$ , SCLK, and $SEP_{IN}$	$0.8 V_{DD1}$		$V_{DD1} + 0.3$	V
Input low-level voltage	$V_{IL}$	$\overline{CS}$ , SIN, $\overline{RST}$ , SCLK, and $SEP_{IN}$	$V_{SS} - 0.3$		$0.2 V_{DD1}$	V
Composite video input voltage	$V_{IN1}$	$CV_{IN}$		2 Vp-p		V
	$V_{IN2}$	$SYN_{IN}$		2 Vp-p	2.5 Vp-p	V
Oscillator frequency	$f_{OSC1}$	Crystal oscillator pins (NTSC: 2fsc mode)		7.15909		MHz
	$f_{OSC2}$	Crystal oscillator pins (NTSC: 4fsc mode)		14.31818		MHz
	$f_{OSC3}$	Crystal oscillator pins (PAL: 4fsc mode)		17.73447		MHz
	$f_{OSC4}$	Crystal oscillator pins (PAL-M: 4fsc mode)		14.30244		MHz
	$f_{OSC5}$	Crystal oscillator pins (PAL-N: 4fsc mode)		14.32822		MHz
	$f_{OSC6}$	LC oscillator pin (When an LC oscillator is used)		5	7	11

#### Electrical Characteristics at $T_a = -30$ to $+70^\circ\text{C}$ , $V_{DD1} = 5$ V unless otherwise specified

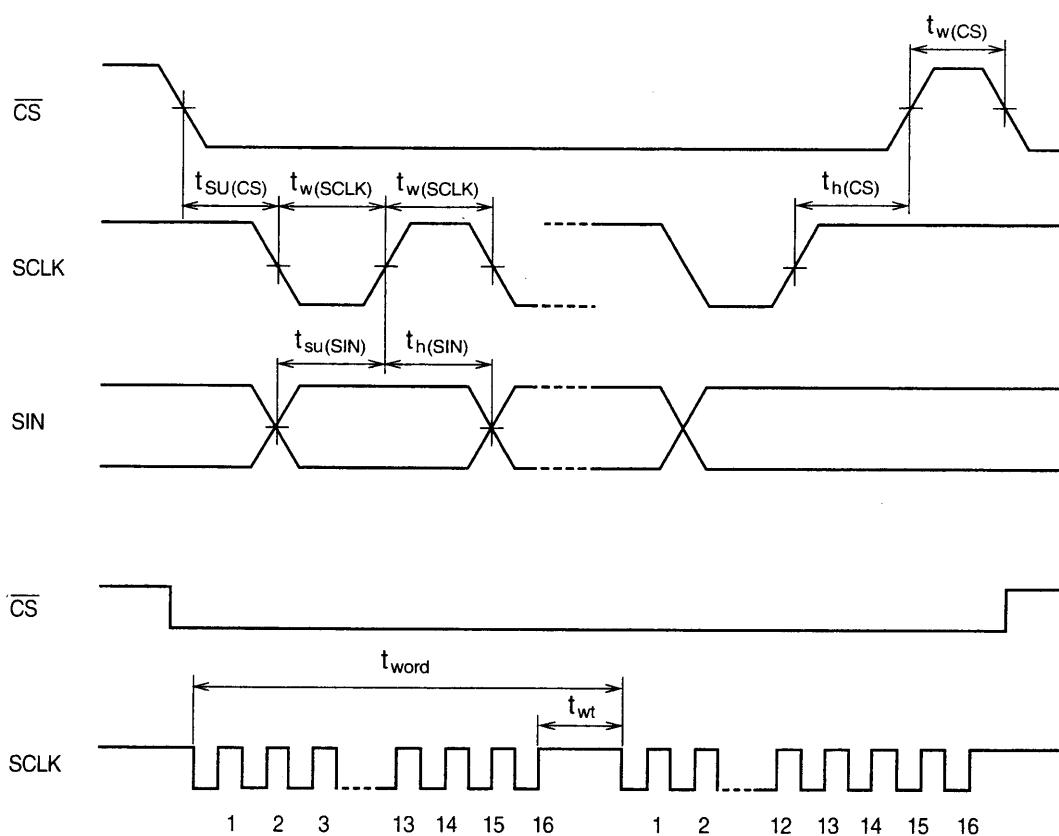
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output off leakage current	$I_{leak}$	$CV_{OUT}$			10	$\mu\text{A}$
Output high-level voltage	$V_{OH1}$	$SEP_{OUT}$ : $V_{DD1} = 4.5$ V, $I_{OH} = -1.0$ mA	3.5			V
Output low-level voltage	$V_{OL1}$	$SEP_{OUT}$ : $V_{DD1} = 4.5$ V, $I_{OL} = 1.0$ mA			1.0	V
Input current	$I_{IH}$	$\overline{CS}$ , SIN, $\overline{RST}$ , SCLK, and $SEP_{IN}$ : $V_{IN} = V_{DD1}$			1	$\mu\text{A}$
	$I_{IL}$	$OSC_{IN}$ : $V_{IN} = V_{SS}$	-1			$\mu\text{A}$
Operating current drain	$I_{DD1}$	$V_{DD1}$ : All outputs open, Xtal: 17.734MHz, LC = 7MHz			10	mA
	$I_{DD2}$	$V_{DD2}$ : $V_{DD2} = 5.0$ V			15	mA

## LC74751

### Timing Characteristics at $T_a = -30$ to $+70^\circ\text{C}$ , $V_{DD1} = 5 \pm 0.5\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	$t_{w(\text{SCLK})}$	SCLK	200			ns
	$t_{w(\text{CS})}$	$\overline{\text{CS}}$ (the period when $\overline{\text{CS}}$ is high)	1			$\mu\text{s}$
Data setup time	$t_{\text{SU}(\text{CS})}$	$\overline{\text{CS}}$	200			ns
	$t_{\text{SU}(\text{SIN})}$	SIN	200			ns
Data hold time	$t_{\text{H}(\text{CS})}$	$\overline{\text{CS}}$	2			$\mu\text{s}$
	$t_{\text{H}(\text{SIN})}$	SIN	200			ns
One-word write time	$t_{\text{word}}$	The time to write 16 bits of data	10			$\mu\text{s}$
	$t_{\text{wt}}$	The time to write data to RAM	1			$\mu\text{s}$

### Serial Data Input Timing



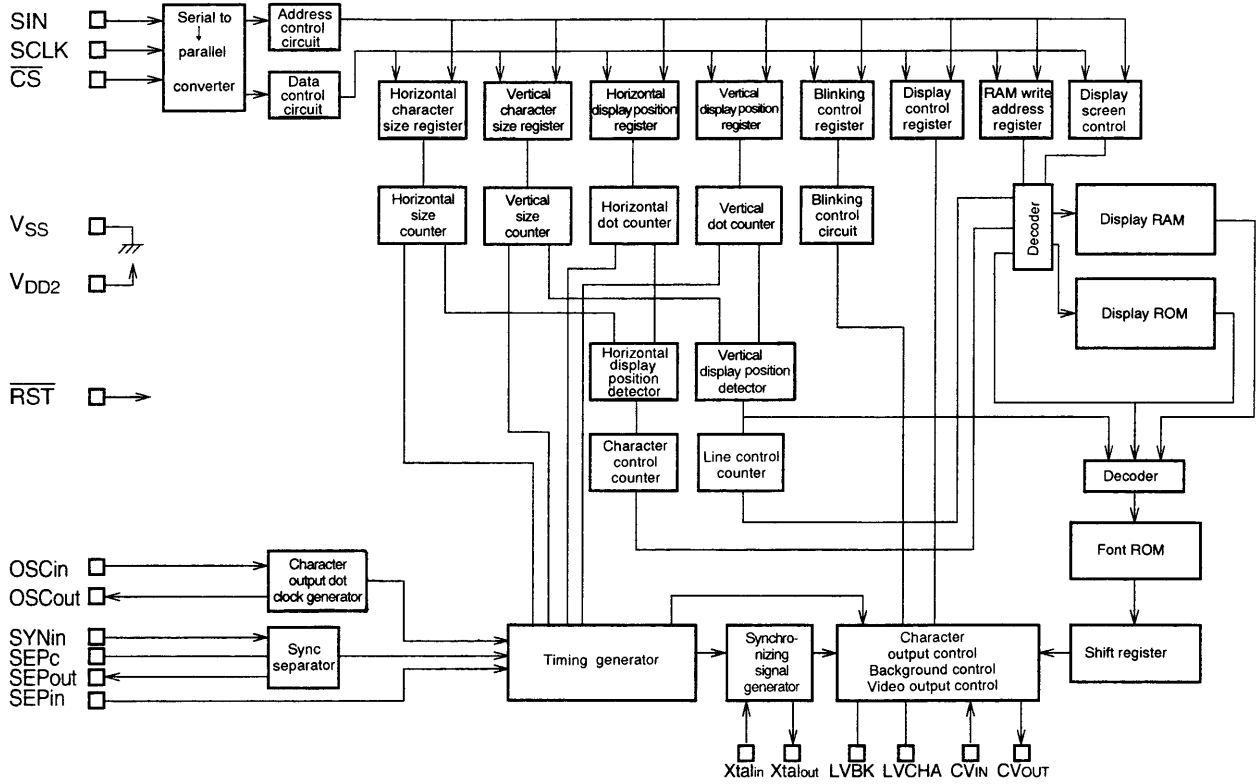
A05638

## LC74751

### Pin Functions

Pin no.	Pin	Function	Notes
1	V <sub>SS</sub>	Ground	Ground (digital system ground)
2	Xtal <sub>IN</sub>	Crystal oscillator	Connections for the crystal and capacitors used to form the crystal oscillator for generating internal synchronizing signals.
3	Xtal <sub>OUT</sub>		
4	TEST	Test output	Test data output
5	RST	Reset input	System reset input (This input has hysteresis characteristics.)
6	SCLK	Clock input	Clock input for the serial data input function (This input has hysteresis characteristics.)
7	SIN	Data input	Serial data input (This input has hysteresis characteristics.) Data is input in 16-bit units.
8	CS	Enable input	Serial data input enable input (This input has hysteresis characteristics.) Serial data input is enabled when this pin is low.
9	LVBK	Blanking level adjustment input	Level input signal used to adjust the blanking level.
10	LVCHA	Character level adjustment input	Level input signal used to adjust the character level.
11	V <sub>DD2</sub>	Power supply	Composite video signal adjustment power supply (analog system power supply)
12	CV <sub>OUT</sub>	Video signal output	Composite video signal output
13	NC		This pin must be either connected to ground or left open.
14	CV <sub>IN</sub>	Video signal input	Composite video signal input
15	V <sub>DD1</sub>	Power supply	Power supply (+5 V)
16	SYN <sub>IN</sub>	Sync separator circuit input	Input to the composite sync signal sync separator circuit
17	SEP <sub>C</sub>	Sync separator circuit adjustment	Sync separator circuit adjustment
18	SEP <sub>OUT</sub>	Composite sync signal output	Sync separator circuit composite sync signal output
19	SEP <sub>IN</sub>	Vertical synchronizing signal input	Connect an integration circuit between the SEP <sub>OUT</sub> pin and this pin, which inputs the vertical synchronizing signal, to integrate the output signal from the SEP <sub>OUT</sub> pin.
20	OSC <sub>OUT</sub>	LC oscillator	Connections for the coil and capacitor that form the oscillator used to generate the character output dot clock.
21	OSC <sub>IN</sub>		
22	V <sub>DD1</sub>	Power supply (+5 V)	Power supply (+5 V)

**System Block Diagram**



A05639

**Display Screen Structure**

The display mode has a 24-character by 12-row format.

The maximum number of characters that can be displayed is 288.

When character sizes are enlarged, the maximum number of characters that can be displayed is reduced.

Display ROM (12-line specification) and display RAM (for 176 characters)

- Specify fixed characters in the display line ROM.
- Application programs use the display RAM to specify characters for sections of the display in which the characters change.

		← 24 characters →																							
12 lines		00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
		24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71
		72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
		96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119
		120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
		144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167
		168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
		192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215
		216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
		240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263
		264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287

## LC74751

### Memory Organization (display RAM and control RAM)

Both memory addresses and data are 16-bit quantities.

The locations at addresses 000 (000 hexadecimal) to 175 (0AF hexadecimal) hold display memory (RAM) data.

The locations at addresses 176 (0B0 hexadecimal) to 191 (0BF hexadecimal) hold display control register data.

Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Notes
000 (000h)	0	0	0	0	0	0	0	0	ATTR	C6	C5	C4	C3	C2	C1	C0	Display RAM
↓	ATTR									Character code							
175 (0AFh)	0	0	0	0	0	0	0	0	ATTR	C6	C5	C4	C3	C2	C1	C0	
176 (0B0h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the first line
177 (0B1h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the second line
178 (0B2h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the third line
179 (0B3h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the fourth line
180 (0B4h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the fifth line
181 (0B5h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the sixth line
182 (0B6h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the seventh line
183 (0B7h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the eighth line
184 (0B8h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the ninth line
185 (0B9h)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the tenth line
186 (0BAh)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the eleventh line
187 (0BBh)	0	0	0	0	0	ADR A	ADR 9	ADR 8	ADR 7	ADR 6	ADR 5	ADR 4	ADR 3	ADR 2	ADR 1	ADR 0	Display line ROM specification First character in the twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position Horizontal character size
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position Vertical character size
190 (0BEh)	0	0	0	0	INT/ NON	LC/ XTAL	2fsc/ 4fsc	OSC STP	DSP ON	MUTE	SYS RST	SIG MD1	SIG MD0	PHASE 2	PHASE 1	PHASE 0	Video signal and other items
191 (0BFh)	0	0	0	0	TST MOD	VSN SEP	0	BLK 1	BLK 0	RVS ON	BLINK 2	BLINK 1	BLINK 0	EXT/ INT	CBOFF	BCOL	Control register

## LC74751

### Address 188 (OBC hexadecimal)

DA 0 to C	Register	Contents		Notes											
		State	Function												
0	HP0 (LSB)	0	If HS is the horizontal start position then: $HS = T_c \times (4 \sum_{n=0}^5 HP_n)$ Tc: Period of the oscillator connected to OSCIN/OSCOU in operating mode.	The 6 bits HP5:0 specify the horizontal display start position.  The weight of the low order bit is 4·Tc.											
		1													
1	HP1	0													
		1													
2	HP2	0													
		1													
3	HP3	0													
		1													
4	HP4	0													
		1													
5	HP5 (MSB)	0													
		1													
6	HSZ10	0			<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">HSZ10 HSZ11</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 Tc/dot</td> <td style="text-align: center;">2 Tc/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 Tc/dot</td> <td style="text-align: center;">4 Tc/dot</td> </tr> </table>	HSZ10 HSZ11	0	1	0	1 Tc/dot	2 Tc/dot	1	3 Tc/dot	4 Tc/dot	The horizontal character size for line 1
		HSZ10 HSZ11				0	1								
0	1 Tc/dot	2 Tc/dot													
1	3 Tc/dot	4 Tc/dot													
1															
7	HSZ11	0													
		1													
8	HSZ20	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">HSZ20 HSZ21</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 Tc/dot</td> <td style="text-align: center;">2 Tc/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 Tc/dot</td> <td style="text-align: center;">4 Tc/dot</td> </tr> </table>	HSZ20 HSZ21		0	1	0	1 Tc/dot	2 Tc/dot	1	3 Tc/dot	4 Tc/dot	The horizontal character size for line 2	
		HSZ20 HSZ21		0		1									
0	1 Tc/dot	2 Tc/dot													
1	3 Tc/dot	4 Tc/dot													
1															
9	HSZ21	0													
		1													
A	HSZ30	0		<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">HSZ30 HSZ31</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 Tc/dot</td> <td style="text-align: center;">2 Tc/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 Tc/dot</td> <td style="text-align: center;">4 Tc/dot</td> </tr> </table>	HSZ30 HSZ31	0	1	0	1 Tc/dot	2 Tc/dot	1	3 Tc/dot	4 Tc/dot		The horizontal character size for lines 2 through 12
		HSZ30 HSZ31			0	1									
0	1 Tc/dot	2 Tc/dot													
1	3 Tc/dot	4 Tc/dot													
1															
B	HSZ31	0													
		1													

Note: The states of all registers are set to zero when the IC is reset by the  $\overline{RST}$  pin.

## LC74751

### Address 189 (OBD hexadecimal)

DA 0 to C	Register	Contents		Notes										
		State	Function											
0	VP0 (LSB)	0	If VS is the vertical display start position then: $VS = H \times (4 \sum_{n=0}^5 VP_n)$	The 6 bits VP5:0 specify the vertical display start position.  The weight of the low order bit is 4·H.										
		1												
1	VP1	0	H: the horizontal synchronization pulse period											
		1												
2	VP2	0												
		1												
3	VP3	0												
		1												
4	VP4	0												
		1												
5	VP5 (MSB)	0												
		1												
6	VSZ10	0		<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">VSZ10 VSZ11</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 H/dot</td> <td style="text-align: center;">2 H/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 H/dot</td> <td style="text-align: center;">4 H/dot</td> </tr> </table>	VSZ10 VSZ11	0	1	0	1 H/dot	2 H/dot	1	3 H/dot	4 H/dot	The vertical character size for line 1
		VSZ10 VSZ11			0	1								
0	1 H/dot	2 H/dot												
1	3 H/dot	4 H/dot												
1														
7	VSZ11	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">VSZ20 VSZ21</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 H/dot</td> <td style="text-align: center;">2 H/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 H/dot</td> <td style="text-align: center;">4 H/dot</td> </tr> </table>	VSZ20 VSZ21	0	1	0	1 H/dot	2 H/dot	1	3 H/dot	4 H/dot	The vertical character size for line 2	
		VSZ20 VSZ21		0	1									
0	1 H/dot	2 H/dot												
1	3 H/dot	4 H/dot												
1														
8	VSZ20	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">VSZ30 VSZ31</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 H/dot</td> <td style="text-align: center;">2 H/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 H/dot</td> <td style="text-align: center;">4 H/dot</td> </tr> </table>	VSZ30 VSZ31	0	1	0	1 H/dot	2 H/dot	1	3 H/dot	4 H/dot	The vertical character size for lines 3 through 12	
		VSZ30 VSZ31		0	1									
0	1 H/dot	2 H/dot												
1	3 H/dot	4 H/dot												
1														
9	VSZ21	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">VSZ30 VSZ31</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 H/dot</td> <td style="text-align: center;">2 H/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 H/dot</td> <td style="text-align: center;">4 H/dot</td> </tr> </table>	VSZ30 VSZ31	0	1	0	1 H/dot	2 H/dot	1	3 H/dot	4 H/dot		
		VSZ30 VSZ31		0	1									
0	1 H/dot	2 H/dot												
1	3 H/dot	4 H/dot												
1														
A	VSZ30	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">VSZ30 VSZ31</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 H/dot</td> <td style="text-align: center;">2 H/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 H/dot</td> <td style="text-align: center;">4 H/dot</td> </tr> </table>	VSZ30 VSZ31	0	1	0	1 H/dot	2 H/dot	1	3 H/dot	4 H/dot		
		VSZ30 VSZ31		0	1									
0	1 H/dot	2 H/dot												
1	3 H/dot	4 H/dot												
1														
B	VSZ31	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">VSZ30 VSZ31</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1 H/dot</td> <td style="text-align: center;">2 H/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">3 H/dot</td> <td style="text-align: center;">4 H/dot</td> </tr> </table>	VSZ30 VSZ31	0	1	0	1 H/dot	2 H/dot	1	3 H/dot	4 H/dot		
		VSZ30 VSZ31		0	1									
0	1 H/dot	2 H/dot												
1	3 H/dot	4 H/dot												
1														

Note: The states of all registers are set to zero when the IC is reset by the  $\overline{RST}$  pin.



## LC74751

Address 190 (OBE hexadecimal)

DA 0 to C	Register	Contents				Notes																																																
		State	Function																																																			
0	PHASE0	0	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">PHASE2</th> <th rowspan="2">PHASE1</th> <th rowspan="2">PHASE0</th> <th colspan="2">Background color (phase)</th> </tr> <tr> <th>NTSC</th> <th>PAL (PAL-M, N)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td><math>\pi/2</math></td> <td><math>\pm \pi/2</math></td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td><math>\pi</math></td> <td>In phase</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td><math>3\pi/2</math></td> <td><math>\mp \pi/2</math></td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>In phase</td> <td><math>\pm \pi</math></td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td><math>\pi/4</math></td> <td><math>\pm 3\pi/4</math></td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td><math>3\pi/4</math></td> <td><math>\pm \pi/4</math></td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td><math>5\pi/4</math></td> <td><math>\mp \pi/4</math></td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td><math>7\pi/4</math></td> <td><math>\pm 3\pi/4</math></td> </tr> </tbody> </table>				PHASE2	PHASE1	PHASE0	Background color (phase)		NTSC	PAL (PAL-M, N)	0	0	0	$\pi/2$	$\pm \pi/2$	0	0	1	$\pi$	In phase	0	1	0	$3\pi/2$	$\mp \pi/2$	0	1	1	In phase	$\pm \pi$	1	0	0	$\pi/4$	$\pm 3\pi/4$	1	0	1	$3\pi/4$	$\pm \pi/4$	1	1	0	$5\pi/4$	$\mp \pi/4$	1	1	1	$7\pi/4$	$\pm 3\pi/4$	Background color The phase of the background color with respect to the color burst signal.
		PHASE2								PHASE1	PHASE0	Background color (phase)																																										
NTSC	PAL (PAL-M, N)																																																					
0	0	0					$\pi/2$	$\pm \pi/2$																																														
0	0	1					$\pi$	In phase																																														
0	1	0					$3\pi/2$	$\mp \pi/2$																																														
0	1	1					In phase	$\pm \pi$																																														
1	0	0					$\pi/4$	$\pm 3\pi/4$																																														
1	0	1					$3\pi/4$	$\pm \pi/4$																																														
1	1	0					$5\pi/4$	$\mp \pi/4$																																														
1	1	1	$7\pi/4$	$\pm 3\pi/4$																																																		
1	PHASE1	0																																																				
1	PHASE1	1																																																				
		0																																																				
2	PHASE2	0																																																				
		1																																																				
3	SIGMD0	0	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SIGMD1</th> <th>SIGMD0</th> <th>Signal format</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>NTSC</td> </tr> <tr> <td>0</td> <td>1</td> <td>PAL</td> </tr> <tr> <td>1</td> <td>0</td> <td>PAL-M</td> </tr> <tr> <td>1</td> <td>1</td> <td>PAL-N</td> </tr> </tbody> </table>				SIGMD1	SIGMD0	Signal format	0	0	NTSC	0	1	PAL	1	0	PAL-M	1	1	PAL-N																																	
		SIGMD1					SIGMD0	Signal format																																														
0	0	NTSC																																																				
0	1	PAL																																																				
1	0	PAL-M																																																				
1	1	PAL-N																																																				
1																																																						
4	SIGMD1	0																																																				
		1																																																				
5	SYRST	0					The IC is reset by a low level on the $\overline{CS}$ pin, and the reset state is cleared by a high level on that pin.																																															
		1	Resets all registers and turns display off.																																																			
6	MUTE	0	Normal output																																																			
		1	$CV_{IN}$ is cut and $CV_{OUT}$ is fixed at the pedestal level.																																																			
7	DSPON	0	Character display off																																																			
		1	Character display on																																																			
8	OSCSTP	0	Crystal oscillator and LC oscillator circuits are not stopped.				Only valid in external synchronization mode when character display is off.																																															
		1	Stops the crystal oscillator and LC oscillator circuits.																																																			
9	$\overline{2fsc}/$ $4fsc/$	0	Clock frequency: 2fsc				Crystal oscillator circuit frequency																																															
		1	Clock frequency: 4fsc																																																			
A	$\overline{LC}/$ XTAL	0	The LC oscillator is used for the dot clock.				The $OSC_{IN}$ pin must be tied to $V_{DD}$ if the LC oscillator circuit is not used.																																															
		1	The crystal oscillator is used for the dot clock.																																																			
B	$\overline{INT}/$ NON	0	Interlaced (262.5 H per field: NTSC, 312.5 H per field: PAL)				Switches interlaced and noninterlaced display.																																															
		1	Noninterlaced (263 H per field: NTSC, 313 H per field: PAL)																																																			

Note: The states of all registers are set to zero when the IC is reset by the  $\overline{RST}$  pin.

## LC74751

Address 191 (OBF hexadecimal)

DA 0 to C	Register	Contents		Notes									
		State	Function										
0	BCOL	0	Background color provided (only valid in internal synchronization mode)										
		1	No background color (Only the background level is set)										
1	CBOFF	0	The burst signal is always output.										
		1	The burst signal is not output when BCOL is high.										
2	$\overline{\text{EXT}}/\text{INT}$	0	External synchronization	Switches between external and internal sources for the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ signals.									
		1	Internal synchronization										
3	BLINK0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">BLINK0 BLINK1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Blinking off</td> <td style="text-align: center;">25% duty</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">50% duty</td> <td style="text-align: center;">75% duty</td> </tr> </table>	BLINK0 BLINK1	0	1	0	Blinking off	25% duty	1	50% duty	75% duty	Changes the blinking duty ratio.
BLINK0 BLINK1	0	1											
0	Blinking off	25% duty											
1	50% duty	75% duty											
1													
4	BLINK1	0											
		1											
5	BLINK2	0	Blinking period: 0.5 s	Changes the blinking period.									
		1	Blinking period: 1.0 s										
6	RVSON	0	Reverse video off										
		1	Reverse video on										
7	BLK0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">BLK0 BLK1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Blinking off</td> <td style="text-align: center;">Character size</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">Frame size</td> <td style="text-align: center;">Whole area size</td> </tr> </table>	BLK0 BLK1	0	1	0	Blinking off	Character size	1	Frame size	Whole area size	Changes the blanking size
BLK0 BLK1	0	1											
0	Blinking off	Character size											
1	Frame size	Whole area size											
1													
8	BLK1	0											
		1											
9	—	0											
		1											
A	VSNSEP	0	External V input used ( $\text{SEP}_{\text{IN}}$ : pin 19)	Selects V input when superimpose mode is used.									
		1	Internal V separation circuit used										
B	TSTMOD	0	Normal operating mode	This bit must be set to 0.									
		1	Test mode										

Note: The states of all registers are set to zero when the IC is reset by the  $\overline{\text{RST}}$  pin.

## LC74751

### Memory (Display ROM) Organization

This memory has addresses ranging from 0 (000 hexadecimal) to 1535 (5FF hexadecimal).

Data has 8 bits.

Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Notes
000 (000h)	0	0	0	0	0	0	0	0	ROM/ RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character in the first line
↓																	
0023 (017h)	0	0	0	0	0	0	0	0	ROM/ RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: 24th character in the first line
0024 (018h)	0	0	0	0	0	0	0	0	ROM/ RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character in the second line
↓																	
↓																	
1535 (5FFh)	0	0	0	0	0	0	0	0	ROM/ RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: 24th character in the 64th line

ROM/  
RAM      Character code

DA 0 to 8	Register	Contents		Notes		
		State	Function			
0	ADR0	0	Specifies an address in character ROM. When specifying display control RAM, DA7 must be set to 1 and ADR0 to ADR6 must be set to 0. The address specification range for character ROM is 0 to 127 (7F hexadecimal).			
		1				
1	ADR1	0				
		1				
2	ADR2	0				
		1				
3	ADR3	0				
		1				
4	ADR4	0				
		1				
5	ADR5	0				
		1				
6	ADR6	0				
		1				
7	ROM/ RAM	0			Data is read directly from character ROM.	
		1			Data is read from character ROM through RAM.	

## Display Line ROM: Line Address Table

Line no.	Address	Line no.	Address
Line 1	000 <sub>HEX</sub> (0000)	Line 33	300 <sub>HEX</sub> (0768)
Line 2	018 <sub>HEX</sub> (0024)	Line 34	318 <sub>HEX</sub> (0792)
Line 3	030 <sub>HEX</sub> (0048)	Line 35	330 <sub>HEX</sub> (0816)
Line 4	048 <sub>HEX</sub> (0072)	Line 36	348 <sub>HEX</sub> (0840)
Line 5	060 <sub>HEX</sub> (0096)	Line 37	360 <sub>HEX</sub> (0864)
Line 6	078 <sub>HEX</sub> (0120)	Line 38	378 <sub>HEX</sub> (0888)
Line 7	090 <sub>HEX</sub> (0144)	Line 39	390 <sub>HEX</sub> (0912)
Line 8	0A8 <sub>HEX</sub> (0168)	Line 40	3A8 <sub>HEX</sub> (0936)
Line 9	0C0 <sub>HEX</sub> (0129)	Line 41	3C0 <sub>HEX</sub> (0960)
Line 10	0D8 <sub>HEX</sub> (0216)	Line 42	3D8 <sub>HEX</sub> (0984)
Line 11	0F0 <sub>HEX</sub> (0240)	Line 43	3F0 <sub>HEX</sub> (1008)
Line 12	108 <sub>HEX</sub> (0264)	Line 44	408 <sub>HEX</sub> (1032)
Line 13	120 <sub>HEX</sub> (0288)	Line 45	420 <sub>HEX</sub> (1056)
Line 14	138 <sub>HEX</sub> (0312)	Line 46	438 <sub>HEX</sub> (1080)
Line 15	150 <sub>HEX</sub> (0336)	Line 47	450 <sub>HEX</sub> (1104)
Line 16	168 <sub>HEX</sub> (0360)	Line 48	468 <sub>HEX</sub> (1128)
Line 17	180 <sub>HEX</sub> (0384)	Line 49	480 <sub>HEX</sub> (1152)
Line 18	198 <sub>HEX</sub> (0408)	Line 50	498 <sub>HEX</sub> (1176)
Line 19	1B0 <sub>HEX</sub> (0432)	Line 51	4B0 <sub>HEX</sub> (1200)
Line 20	1C8 <sub>HEX</sub> (0456)	Line 52	4C8 <sub>HEX</sub> (1224)
Line 21	1E0 <sub>HEX</sub> (0480)	Line 53	4E0 <sub>HEX</sub> (1248)
Line 22	1F8 <sub>HEX</sub> (0504)	Line 54	4F8 <sub>HEX</sub> (1272)
Line 23	210 <sub>HEX</sub> (0528)	Line 55	510 <sub>HEX</sub> (1296)
Line 24	228 <sub>HEX</sub> (0552)	Line 56	528 <sub>HEX</sub> (1320)
Line 25	240 <sub>HEX</sub> (0576)	Line 57	540 <sub>HEX</sub> (1344)
Line 26	258 <sub>HEX</sub> (0600)	Line 58	558 <sub>HEX</sub> (1368)
Line 27	270 <sub>HEX</sub> (0624)	Line 59	570 <sub>HEX</sub> (1392)
Line 28	288 <sub>HEX</sub> (0648)	Line 60	588 <sub>HEX</sub> (1416)
Line 29	2A0 <sub>HEX</sub> (0672)	Line 61	5A0 <sub>HEX</sub> (1440)
Line 30	2B8 <sub>HEX</sub> (0696)	Line 62	5B8 <sub>HEX</sub> (1464)
Line 31	2D0 <sub>HEX</sub> (0720)	Line 63	5D0 <sub>HEX</sub> (1488)
Line 32	2E8 <sub>HEX</sub> (0744)	Line 64	5E8 <sub>HEX</sub> (1512)

**Display Screen Structure (Display Example)**

Specify the display of line 12 for display line ROM (64 lines).

From within line ROM, specify display control RAM for the sections where the characters are variable.

The addresses in display control RAM are automatically allocated in display order from 0 to 175 (AF hexadecimal).



Items enclosed in thick lines specify characters in display control RAM, and

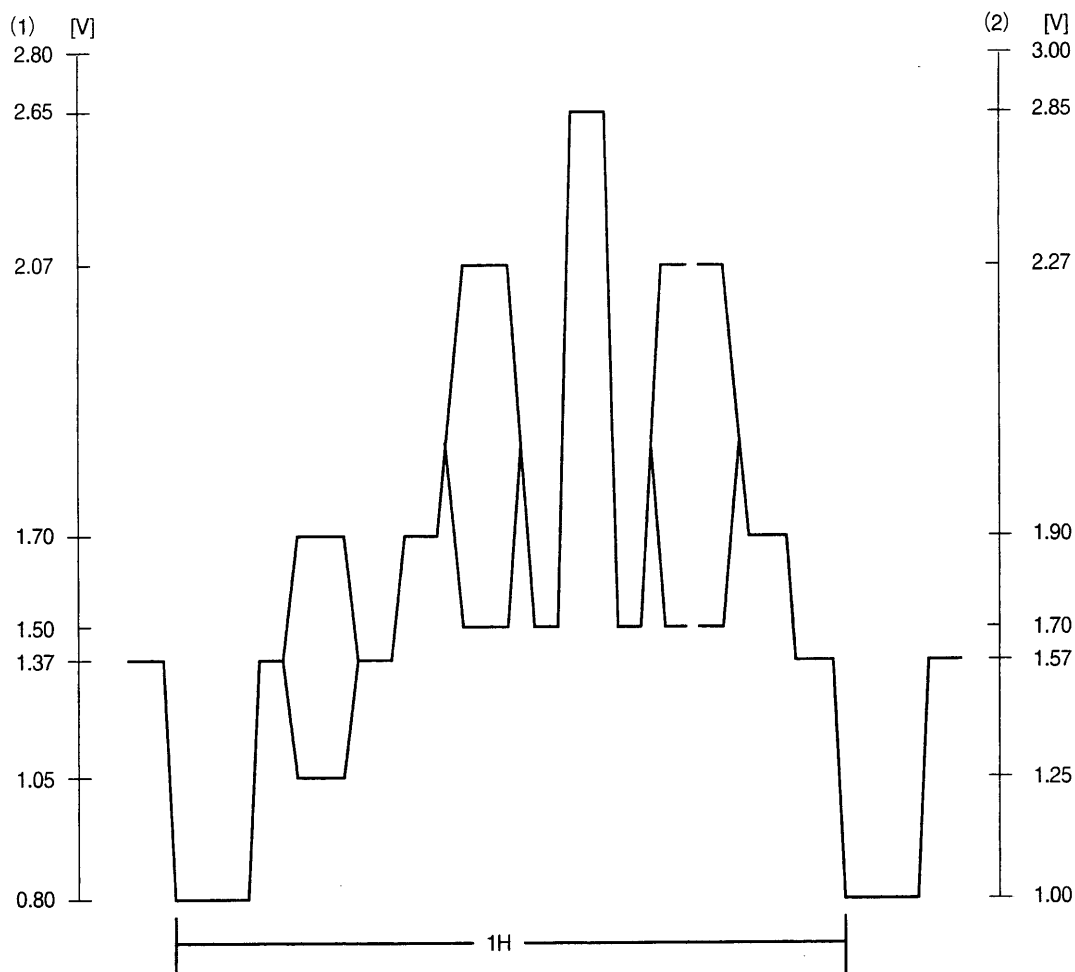


items enclosed in thin lines are character specified in line ROM.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
1	ROM 000 00h	ROM 001 01h	ROM 002 02h	ROM 003 03h	ROM 004 04h	ROM 005 05h	ROM 006 06h	ROM 007 07h	ROM 008 08h	ROM 009 09h	ROM 010 0Ah	ROM 011 0Bh	ROM 012 0Ch	ROM 013 0Dh	ROM 014 0Eh	ROM 015 0Fh	RAM 000 00h	RAM 001 01h	RAM 002 02h	RAM 003 03h	RAM 004 04h	RAM 005 05h	ROM 022 16h	ROM 023 17h																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
2	ROM 024 18h	RAM 006 06h	RAM 007 07h	RAM 008 08h	RAM 009 09h	ROM 029 1Dh	ROM 030 1Eh	ROM 031 1Fh	ROM 032 20h	ROM 033 21h	RAM 00A 0Ah	RAM 00B 0Bh	RAM 00C 0Ch	RAM 00D 0Dh	RAM 00E 0Eh	RAM 00F 0Fh	ROM 040 28h	ROM 041 29h	ROM 042 2Ah	ROM 043 2Bh	ROM 044 2Ch	ROM 045 2Dh	ROM 046 2Eh	ROM 047 2Fh																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
3	ROM 048 18h	RAM 016 10h	RAM 017 11h	RAM 018 12h	RAM 019 13h	RAM 020 14h	ROM 054 36h	ROM 055 37h	ROM 056 38h	ROM 057 39h	RAM 021 15h	RAM 022 16h	RAM 023 17h	RAM 024 18h	RAM 025 19h	RAM 026 1Ah	RAM 027 1Bh	RAM 028 1Ch	RAM 029 1Dh	RAM 02A 1Eh	ROM 068 44h	ROM 069 45h	ROM 070 46h	ROM 071 47h																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
4	ROM 072 48h	ROM 073 49h	ROM 074 4Ah	ROM 075 4Bh	ROM 076 4Ch	RAM 021 1Fh	RAM 022 20h	RAM 023 21h	RAM 024 22h	RAM 025 23h	RAM 026 24h	RAM 027 25h	RAM 028 26h	RAM 029 27h	RAM 02A 28h	RAM 02B 29h	RAM 02C 2Ah	RAM 02D 2Bh	RAM 02E 2Ch	RAM 02F 2Dh	ROM 091 55h	ROM 092 56h	ROM 093 57h	ROM 094 58h	ROM 095 59h																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																					
5	ROM 096 60h	RAM 041 29h	RAM 042 2Ah	RAM 043 2Bh	RAM 044 2Ch	RAM 045 2Dh	RAM 046 2Eh	RAM 047 2Fh	RAM 048 30h	ROM 105 69h	RAM 049 31h	RAM 050 32h	RAM 051 33h	RAM 052 34h	RAM 053 35h	RAM 054 36h	RAM 055 37h	RAM 056 38h	RAM 057 39h	RAM 058 3Ah	RAM 059 3Bh	ROM 114 72h	ROM 115 73h	ROM 116 74h	ROM 117 75h	ROM 118 76h	ROM 119 77h																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
6	ROM 120 78h	RAM 055 3Fh	RAM 056 40h	RAM 057 41h	RAM 058 42h	RAM 059 43h	RAM 060 44h	RAM 061 45h	RAM 062 46h	RAM 063 47h	RAM 064 48h	RAM 065 49h	RAM 066 4Ah	RAM 067 4Bh	RAM 068 4Ch	RAM 069 4Dh	RAM 070 4Eh	RAM 071 4Fh	RAM 072 50h	RAM 073 51h	RAM 074 52h	RAM 075 53h	RAM 076 54h	RAM 077 55h	RAM 078 56h	RAM 079 57h	RAM 080 58h	RAM 081 59h	RAM 082 5Ah	RAM 083 5Bh	RAM 084 5Ch	RAM 085 5Dh	RAM 086 5Eh	RAM 087 5Fh	RAM 088 60h	RAM 089 61h	RAM 090 62h	RAM 091 63h	RAM 092 64h	RAM 093 65h	RAM 094 66h	RAM 095 67h	RAM 096 68h	RAM 097 69h	RAM 098 6Ah	RAM 099 6Bh	RAM 100 6Ch	RAM 101 6Dh	RAM 102 6Eh	RAM 103 6Fh	RAM 104 70h	RAM 105 71h	RAM 106 72h	RAM 107 73h	RAM 108 74h	RAM 109 75h	RAM 110 76h	RAM 111 77h	RAM 112 78h	RAM 113 79h	RAM 114 7Ah	RAM 115 7Bh	RAM 116 7Ch	RAM 117 7Dh	RAM 118 7Eh	RAM 119 7Fh	RAM 120 80h	RAM 121 81h	RAM 122 82h	RAM 123 83h	RAM 124 84h	RAM 125 85h	RAM 126 86h	RAM 127 87h	RAM 128 88h	RAM 129 89h	RAM 130 8Ah	RAM 131 8Bh	RAM 132 8Ch	RAM 133 8Dh	RAM 134 8Eh	RAM 135 8Fh	RAM 136 90h	RAM 137 91h	RAM 138 92h	RAM 139 93h	RAM 140 94h	RAM 141 95h	RAM 142 96h	RAM 143 97h	RAM 144 98h	RAM 145 99h	RAM 146 9Ah	RAM 147 9Bh	RAM 148 9Ch	RAM 149 9Dh	RAM 150 9Eh	RAM 151 9Fh	RAM 152 A0h	RAM 153 A1h	RAM 154 A2h	RAM 155 A3h	RAM 156 A4h	RAM 157 A5h	RAM 158 A6h	RAM 159 A7h	RAM 160 A8h	RAM 161 A9h	RAM 162 AAh	RAM 163 ABh	RAM 164 ACh	RAM 165 ADh	RAM 166 AEh	RAM 167 AFh	RAM 168 B0h	RAM 169 B1h	RAM 170 B2h	RAM 171 B3h	RAM 172 B4h	RAM 173 B5h	RAM 174 B6h	RAM 175 B7h	RAM 176 B8h	RAM 177 B9h	RAM 178 BAh	RAM 179 BAh	RAM 180 BAh	RAM 181 BAh	RAM 182 BAh	RAM 183 BAh	RAM 184 BAh	RAM 185 BAh	RAM 186 BAh	RAM 187 BAh	RAM 188 BAh	RAM 189 BAh	RAM 190 BAh	RAM 191 BAh	RAM 192 BAh	RAM 193 BAh	RAM 194 BAh	RAM 195 BAh	RAM 196 BAh	RAM 197 BAh	RAM 198 BAh	RAM 199 BAh	RAM 200 BAh	RAM 201 BAh	RAM 202 BAh	RAM 203 BAh	RAM 204 BAh	RAM 205 BAh	RAM 206 BAh	RAM 207 BAh	RAM 208 BAh	RAM 209 BAh	RAM 210 BAh	RAM 211 BAh	RAM 212 BAh	RAM 213 BAh	RAM 214 BAh	RAM 215 BAh	RAM 216 BAh	RAM 217 BAh	RAM 218 BAh	RAM 219 BAh	RAM 220 BAh	RAM 221 BAh	RAM 222 BAh	RAM 223 BAh	RAM 224 BAh	RAM 225 BAh	RAM 226 BAh	RAM 227 BAh	RAM 228 BAh	RAM 229 BAh	RAM 230 BAh	RAM 231 BAh	RAM 232 BAh	RAM 233 BAh	RAM 234 BAh	RAM 235 BAh	RAM 236 BAh	RAM 237 BAh	RAM 238 BAh	RAM 239 BAh	RAM 240 BAh	RAM 241 BAh	RAM 242 BAh	RAM 243 BAh	RAM 244 BAh	RAM 245 BAh	RAM 246 BAh	RAM 247 BAh	RAM 248 BAh	RAM 249 BAh	RAM 250 BAh	RAM 251 BAh	RAM 252 BAh	RAM 253 BAh	RAM 254 BAh	RAM 255 BAh	RAM 256 BAh	RAM 257 BAh	RAM 258 BAh	RAM 259 BAh	RAM 260 BAh	RAM 261 BAh	RAM 262 BAh	RAM 263 BAh	RAM 264 BAh	RAM 265 BAh	RAM 266 BAh	RAM 267 BAh	RAM 268 BAh	RAM 269 BAh	RAM 270 BAh	RAM 271 BAh	RAM 272 BAh	RAM 273 BAh	RAM 274 BAh	RAM 275 BAh	RAM 276 BAh	RAM 277 BAh	RAM 278 BAh	RAM 279 BAh	RAM 280 BAh	RAM 281 BAh	RAM 282 BAh	RAM 283 BAh	RAM 284 BAh	RAM 285 BAh	RAM 286 BAh	RAM 287 BAh	RAM 288 BAh	RAM 289 BAh	RAM 290 BAh	RAM 291 BAh	RAM 292 BAh	RAM 293 BAh	RAM 294 BAh	RAM 295 BAh	RAM 296 BAh	RAM 297 BAh	RAM 298 BAh	RAM 299 BAh	RAM 300 BAh	RAM 301 BAh	RAM 302 BAh	RAM 303 BAh	RAM 304 BAh	RAM 305 BAh	RAM 306 BAh	RAM 307 BAh	RAM 308 BAh	RAM 309 BAh	RAM 310 BAh	RAM 311 BAh	RAM 312 BAh	RAM 313 BAh	RAM 314 BAh	RAM 315 BAh	RAM 316 BAh	RAM 317 BAh	RAM 318 BAh	RAM 319 BAh	RAM 320 BAh	RAM 321 BAh	RAM 322 BAh	RAM 323 BAh	RAM 324 BAh	RAM 325 BAh	RAM 326 BAh	RAM 327 BAh	RAM 328 BAh	RAM 329 BAh	RAM 330 BAh	RAM 331 BAh	RAM 332 BAh	RAM 333 BAh	RAM 334 BAh	RAM 335 BAh	RAM 336 BAh	RAM 337 BAh	RAM 338 BAh	RAM 339 BAh	RAM 340 BAh	RAM 341 BAh	RAM 342 BAh	RAM 343 BAh	RAM 344 BAh	RAM 345 BAh	RAM 346 BAh	RAM 347 BAh	RAM 348 BAh	RAM 349 BAh	RAM 350 BAh	RAM 351 BAh	RAM 352 BAh	RAM 353 BAh	RAM 354 BAh	RAM 355 BAh	RAM 356 BAh	RAM 357 BAh	RAM 358 BAh	RAM 359 BAh	RAM 360 BAh	RAM 361 BAh	RAM 362 BAh	RAM 363 BAh	RAM 364 BAh	RAM 365 BAh	RAM 366 BAh	RAM 367 BAh	RAM 368 BAh	RAM 369 BAh	RAM 370 BAh	RAM 371 BAh	RAM 372 BAh	RAM 373 BAh	RAM 374 BAh	RAM 375 BAh	RAM 376 BAh	RAM 377 BAh	RAM 378 BAh	RAM 379 BAh	RAM 380 BAh	RAM 381 BAh	RAM 382 BAh	RAM 383 BAh	RAM 384 BAh	RAM 385 BAh	RAM 386 BAh	RAM 387 BAh	RAM 388 BAh	RAM 389 BAh	RAM 390 BAh	RAM 391 BAh	RAM 392 BAh	RAM 393 BAh	RAM 394 BAh	RAM 395 BAh	RAM 396 BAh	RAM 397 BAh	RAM 398 BAh	RAM 399 BAh	RAM 400 BAh	RAM 401 BAh	RAM 402 BAh	RAM 403 BAh	RAM 404 BAh	RAM 405 BAh	RAM 406 BAh	RAM 407 BAh	RAM 408 BAh	RAM 409 BAh	RAM 410 BAh	RAM 411 BAh	RAM 412 BAh	RAM 413 BAh	RAM 414 BAh	RAM 415 BAh	RAM 416 BAh	RAM 417 BAh	RAM 418 BAh	RAM 419 BAh	RAM 420 BAh	RAM 421 BAh	RAM 422 BAh	RAM 423 BAh	RAM 424 BAh	RAM 425 BAh	RAM 426 BAh	RAM 427 BAh	RAM 428 BAh	RAM 429 BAh	RAM 430 BAh	RAM 431 BAh	RAM 432 BAh	RAM 433 BAh	RAM 434 BAh	RAM 435 BAh	RAM 436 BAh	RAM 437 BAh	RAM 438 BAh	RAM 439 BAh	RAM 440 BAh	RAM 441 BAh	RAM 442 BAh	RAM 443 BAh	RAM 444 BAh	RAM 445 BAh	RAM 446 BAh	RAM 447 BAh	RAM 448 BAh	RAM 449 BAh	RAM 450 BAh	RAM 451 BAh	RAM 452 BAh	RAM 453 BAh	RAM 454 BAh	RAM 455 BAh	RAM 456 BAh	RAM 457 BAh	RAM 458 BAh	RAM 459 BAh	RAM 460 BAh	RAM 461 BAh	RAM 462 BAh	RAM 463 BAh	RAM 464 BAh	RAM 465 BAh	RAM 466 BAh	RAM 467 BAh	RAM 468 BAh	RAM 469 BAh	RAM 470 BAh	RAM 471 BAh	RAM 472 BAh	RAM 473 BAh	RAM 474 BAh	RAM 475 BAh	RAM 476 BAh	RAM 477 BAh	RAM 478 BAh	RAM 479 BAh	RAM 480 BAh	RAM 481 BAh	RAM 482 BAh	RAM 483 BAh	RAM 484 BAh	RAM 485 BAh	RAM 486 BAh	RAM 487 BAh	RAM 488 BAh	RAM 489 BAh	RAM 490 BAh	RAM 491 BAh	RAM 492 BAh	RAM 493 BAh	RAM 494 BAh	RAM 495 BAh	RAM 496 BAh	RAM 497 BAh	RAM 498 BAh	RAM 499 BAh	RAM 500 BAh	RAM 501 BAh	RAM 502 BAh	RAM 503 BAh	RAM 504 BAh	RAM 505 BAh	RAM 506 BAh	RAM 507 BAh	RAM 508 BAh	RAM 509 BAh	RAM 510 BAh	RAM 511 BAh	RAM 512 BAh	RAM 513 BAh	RAM 514 BAh	RAM 515 BAh	RAM 516 BAh	RAM 517 BAh	RAM 518 BAh	RAM 519 BAh	RAM 520 BAh	RAM 521 BAh	RAM 522 BAh	RAM 523 BAh	RAM 524 BAh	RAM 525 BAh	RAM 526 BAh	RAM 527 BAh	RAM 528 BAh	RAM 529 BAh	RAM 530 BAh	RAM 531 BAh	RAM 532 BAh	RAM 533 BAh	RAM 534 BAh	RAM 535 BAh	RAM 536 BAh	RAM 537 BAh	RAM 538 BAh	RAM 539 BAh	RAM 540 BAh	RAM 541 BAh	RAM 542 BAh	RAM 543 BAh	RAM 544 BAh	RAM 545 BAh	RAM 546 BAh	RAM 547 BAh	RAM 548 BAh	RAM 549 BAh	RAM 550 BAh	RAM 551 BAh	RAM 552 BAh	RAM 553 BAh	RAM 554 BAh	RAM 555 BAh	RAM 556 BAh	RAM 557 BAh	RAM 558 BAh	RAM 559 BAh	RAM 560 BAh	RAM 561 BAh	RAM 562 BAh	RAM 563 BAh	RAM 564 BAh	RAM 565 BAh	RAM 566 BAh	RAM 567 BAh	RAM 568 BAh	RAM 569 BAh	RAM 570 BAh	RAM 571 BAh	RAM 572 BAh	RAM 573 BAh	RAM 574 BAh	RAM 575 BAh	RAM 576 BAh	RAM 577 BAh	RAM 578 BAh	RAM 579 BAh	RAM 580 BAh	RAM 581 BAh	RAM 582 BAh	RAM 583 BAh	RAM 584 BAh	RAM 585 BAh	RAM 586 BAh	RAM 587 BAh	RAM 588 BAh	RAM 589 BAh	RAM 590 BAh	RAM 591 BAh	RAM 592 BAh	RAM 593 BAh	RAM 594 BAh	RAM 595 BAh	RAM 596 BAh	RAM 597 BAh	RAM 598 BAh	RAM 599 BAh	RAM 600 BAh	RAM 601 BAh	RAM 602 BAh	RAM 603 BAh	RAM 604 BAh	RAM 605 BAh	RAM 606 BAh	RAM 607 BAh	RAM 608 BAh	RAM 609 BAh	RAM 610 BAh	RAM 611 BAh	RAM 612 BAh	RAM 613 BAh	RAM 614 BAh	RAM 615 BAh	RAM 616 BAh	RAM 617 BAh	RAM 618 BAh	RAM 619 BAh	RAM 620 BAh	RAM 621 BAh	RAM 622 BAh	RAM 623 BAh	RAM 624 BAh	RAM 625 BAh	RAM 626 BAh	RAM 627 BAh	RAM 628 BAh	RAM 629 BAh	RAM 630 BAh	RAM 631 BAh	RAM 632 BAh	RAM 633 BAh	RAM 634 BAh	RAM 635 BAh	RAM 636 BAh	RAM 637 BAh	RAM 638 BAh	RAM 639 BAh	RAM 640 BAh	RAM 641 BAh	RAM 642 BAh	RAM 643 BAh	RAM 644 BAh	RAM 645 BAh	RAM 646 BAh	RAM 647 BAh	RAM 648 BAh	RAM 649 BAh	RAM 650 BAh	RAM 651 BAh	RAM 652 BAh	RAM 653 BAh	RAM 654 BAh	RAM 655 BAh	RAM 656 BAh	RAM 657 BAh	RAM 658 BAh	RAM 659 BAh	RAM 660 BAh	RAM 661 BAh	RAM 662 BAh	RAM 663 BAh	RAM 664 BAh	RAM 665 BAh	RAM 666 BAh	RAM 667 BAh	RAM 668 BAh	RAM 669 BAh	RAM 670 BAh	RAM 671 BAh	RAM 672 BAh	RAM 673 BAh	RAM 674 BAh	RAM 675 BAh	RAM 676 BAh	RAM 677 BAh	RAM 678 BAh	RAM 679 BAh	RAM 680 BAh	RAM 681 BAh	RAM 682 BAh	RAM 683 BAh	RAM 684 BAh	RAM 685 BAh	RAM 686 BAh	RAM 687 BAh	RAM 688 BAh	RAM 689 BAh	RAM 690 BAh	RAM 6

Composite Video Signal Output Levels (Internally Generated Levels)

CV<sub>OUT</sub> output level waveform (V<sub>DD2</sub> = 5.00 V)

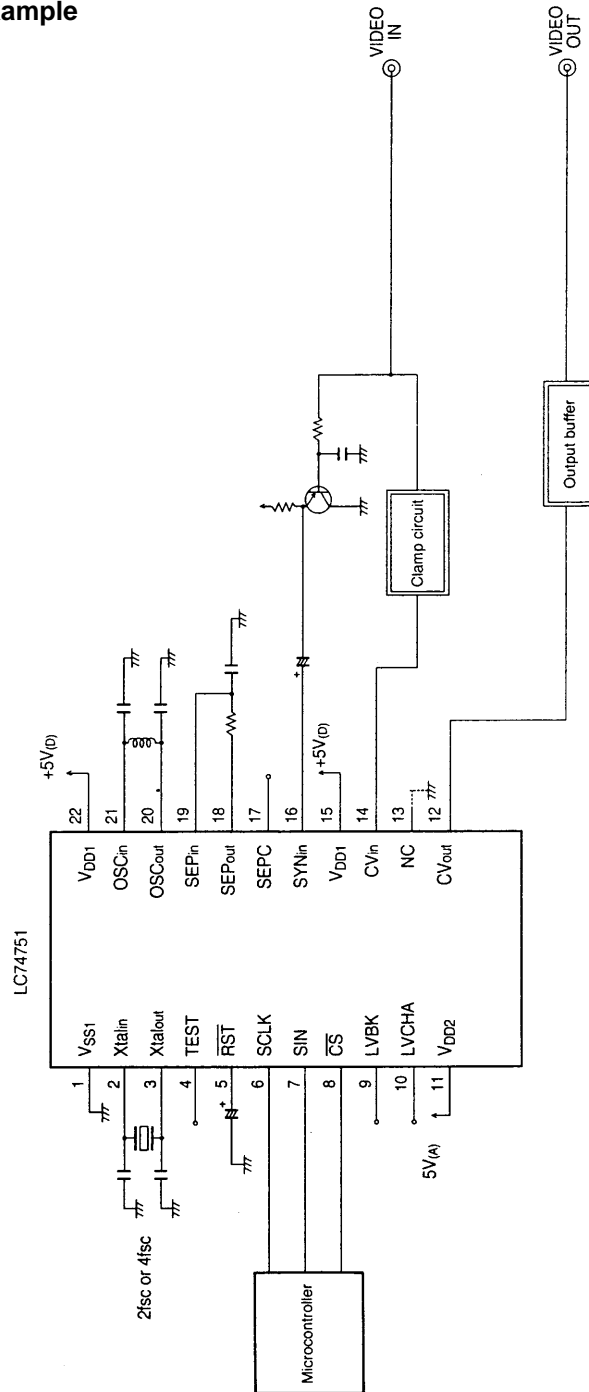


A05641

Output level	Output voltage (1) (V <sub>DC</sub> )	Output voltage (2) (V <sub>DC</sub> )
V <sub>CHA</sub> : Character	2.650	2.875
V <sub>RSH</sub> : Background color high	2.075	2.275
V <sub>CBH</sub> : Color burst high	1.700	1.900
V <sub>RSL</sub> : Background color low	1.500	1.700
V <sub>BK</sub> : Frame	1.500	1.700
V <sub>PD</sub> : Pedestal level	1.375	1.575
V <sub>CBL</sub> : Color burst low	1.050	1.250
V <sub>SN</sub> : Sync	0.800	1.000

V<sub>DD2</sub> = 5.000V<sub>DC</sub>

Application Circuit Example



ACS642

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
  - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of August, 1996. Specifications and information herein are subject to change without notice.